

Development of Micro Phasor Measurement Unit (µ-PMU) to Facilitate Synchrophor Learning at Undergraduate Level

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Abstract

Synchrophasor and Phasor measurement unit (PMU) technology has been widely deployed in electrical power transmission network for protection and state estimation. This technology has also been extended at distribution level mainly in Smartgrids and Microgrids. The increased applications of Synchrophasors had made it necessary to develop trained engineering graduates in the field. In this work, a laboratory prototype of micro PMU (μ PMU) has been developed using a microcontroller board and open source software as per the IEEE standards. The prototype has all the functionalities of commercially available PMU with some compromises on the speed and data transmission rate due to the hardware limitations. Simulated results show that the μ PMU functionalities can be very well demonstrated using the prototype.

Keywords

Phasor Measurement Unit, Synchrophasor, µPMU, ESP-32

Introduction

Synchrophasor technique has been widely deployed in electrical power transmission network for protection and state estimation. Phasor measurement unit (PMU) is the basic building block of syncrophasors, that gathers the time synchronised information of magnitude and phase of electrical quantities [1-3]. In recent years, the increased awareness about green energy sources is changing the structure of the electrical network. Microgrids and Smartgrids are setup to accommodate the distributed renewable energy sources in the power system [4-6]. With this scenario, the concept of synchrophaser has been extended to the distribution network. Micro PMU(μ -PMU) is the device, that is used in distribution network to obtain the synchrophaor parameters at medium/low voltage level.

Looking at the growth of distributed generation and Microgrid, there will be a need for skilled personnel able to undertake roles such as researchers, resource planners, engineers, and technicians in coming years. Therefore, it is important that students should learn the concepts of synchrophasors and PMU. The commercially available proprietary PMUs are based on high computational power processors with high speed communication network to exchange huge data base to phasor data concentrators (PDC). The setup is quite expensive and may not be affordable by the undergraduate level institutions focused primarily on the teaching learning. This work is an attempt to develop low cost till accurate μ -PMU unit for the demonstration of synchrophasor concept to undergraduate students.

Proposed device has provision to calculate magnitude, frequency and phase at low voltage level. A GPS module is used for time-stamping the data in order to have the same time reference, according to the IEEE c37.118.1-2011 standards. Provision is there to send the data to a local server for display and storage. Optional LCD is also provided for the live display of parameters. The archived data can be used for implementing power flow control strategy, system model validation as well as load sharing amongst DG sources. The main features of μ PMU include high sampling frequency of 10 kS/s, use of open source hardware and software platforms and lower cost.

This paper is divided as follows: In initial section, synchrophasor terminologies have been given followed by the development of μ PMU hardware and software in next section. Implementation results are summarised in the later section, while the last section briefs the conclusion and future scope.

Synchrophasor Terminology:

Various terms used in the synchrophasor as per IEEE standard c37.118.1 [7] are as follows

i. Phasor: A complex equivalent of a sinusoidal wave quantity such that the complex modulus is the cosine wave amplitude and the complex angle (in polar form) is the cosine wave phase angle.

ii. Synchronized Phasor or Synchrophasor: A phasor calculated from data samples using a standard time signal as the reference for the measurement.

The representation of sinusoidal waveform commonly used in ac power system analysis is as shown in Equations:

$x(t) = X_{\rm m} \cos \left(\omega t + \varphi\right)$	(1)
The phasor is also represented as	
$X = (X_{\rm m}/\sqrt{2}) e^{j\varphi}$	(2)
$= (X_{\rm m} / \sqrt{2}) (\cos \varphi + i \sin \varphi) = X_{\rm r} + i X_{\rm i}$	

Here the magnitude is the RMS value, $(X_m / \sqrt{2})$, of the waveform and the subscripts r and i signify real and imaginary parts of a complex value in rectangular components. φ is the instantaneous phase angle relative to a cosine function at the nominal system frequency.

iii. Phasor Measurement Unit (PMU): A device that produces synchronized phasor, frequency, and rate of change of frequency (ROCOF) estimates from voltage and/or current signals and a time synchronizing signal.

iv. Frequency and Rate of Change of Frequency (ROCOF): A PMU shall be capable of reporting frequency and ROCOF as per the following standard definitions.

Let a sinusoidal waveform with no phase shift is represented as	
$x(t) = Xm \cos\left[\psi(t)\right]$	(3)
Frequency is defined as	
$f(t) = \frac{1}{2\pi} \frac{d\varphi(t)}{dt}$	(4)
And the ROCOF is defined as	
AE(+)	

 $ROCOF = \frac{df(t)}{dt}$ (5) v. Coordinated Universal Time (UTC): It is the time of day at the Earth's prime meridian (0° longitude). It is distributed by various media, including the Global Positioning System (GPS) system.

vi. Time Tag for Synchrophasor: Synchrophasor measurements shall be tagged with the UTC time corresponding to the time of measurement. This consist of three numbers: a second-of-century (SOC) count, a fraction-of-second (FRACSEC) count, and a message time quality flag. The SOC count is a four (4) byte binary count of seconds from UTC midnight (00:00:00) of January 1, 1970, to the current second. The FRACSEC count is an integer representing the numerator of the FRACSEC with TIME BASE as the denominator.

vii. Data Frame: Data frame is sequence of information transmitted by PMU. The data frame format used in this work is given in Table 1.1.

Sr.	Field	Size (bytes)	Comment
No.			
1	SYNC	2	Sync byte followed by frame type and version number.
2	FRAMESIZE	2	Number of bytes in frame
3	IDCODE	2	Stream source ID number, 16-bit integer,
4	SOC	4	SOC time stamp, for all measurements in frame.
5	FRACSEC	4	Fraction of Second and Time Quality, for all measurements in frame.
6	STAT	2	Bit-mapped flags.
7	PHASORS	6× PHNMR	Phasor estimates, Three phase positive sequence voltage, Three
			phase positive sequence current.
8	FREQ	2	Frequency
9	DFREQ	2	ROCOF
10	CHK	2	Cyclic redundancy check(CRC-CCITT
T-LL 1. DMU D-4- E			

Table 1: PMU Data Frame Format

μ PMU Development

μ PMU requires the hardware as well as the associated firmware. Hardware development mainly consist of development of signal conditioning circuits for voltage and current sensors and GPS circuit interfacing. The proposed µPMU is intended for use at distribution level, where noise is a measure issue. Thus, suitable filters are used to attenuate the high frequency noise. On firmware side, it has been optimised to deal with issue of fixed deadline operations. µ PMU has to complete the tasks in a fixed time frame and jumping of time frame results in serious errors in subsequent data analysis. The hardware and firmware development is discussed in coming paragraphs:

Hardware Development: The hardware development is divided in two parts as of i) voltage and current sensing circuits and ii) GPS based time tracking circuit.

i) Voltage and Current Sensing Circuit: Current and Potential transformer is used for current and voltage sensing. The microcontroller board used in this work has unipolar type analog to digital converter (ADC); thus, to accommodate the negative half of AC signal, an offset of 1.5V is given as shown in fig1.(a). This approach limits the excursion of attenuated AC signal between 0 to 3V. Provision has been done for the measurement of voltage and current of R, Y and B phases.

Zero crossing detector is used to generate pulses synchronised with the zero crossing of fundamental component of system voltage. R phase voltage is attenuated and low pass filtered to extract the 50Hz component. This

signal is given to a comparator to obtain a 50 Hz square wave. System frequency is also measured from this signal and used to verify the results obtained from FFT of the voltage signal.[9] The low pass filter, phase compensator and comparator circuit is shown in fig,1(b)



Fig.1: (a) DC Offset and Signal Conditioning Circuit (b) Low Pass Filter and Zero Crossing Detection

ii) GPS Time Measurement: At the most fundamental level, PMU has two functions. One to keep track of the time and the second to take input and give output at very specific and precise intervals. As per IEEE standard, the precision required is in terms of time of microsecond resolution and that too so accurate, that the drift should be not more than 100 nanoseconds from the atomic clock. As the clock source of such precision is extensive costly, a microsecond resolution clock has been designed and used as a time keeping device.

GPS satellites have multiple atomic clocks on-board to provide with precise time as required for GPS related work. Extraction of atomic clock from GPS signal is much tedious and has huge computational load. To simplify this, a GPS receiver that generates pulse per second (PPS) signal has been used in this work. As soon as controller receives a pulse, 100 microsecond duration pulse is generated. This pulse is exactly synchronized with the GPS satellites atomic time. The pulse is highly accurate and used as time reference to design the clock. The task of generating a clock of microsecond resolution is implemented using ESP32 microcontroller.[8] ESP32 has two cores (core 0 and core 1) that works in parallel. The timer interrupt service routine executes on core 0 of the controller. Circuit arrangement of GPS with ESP32 is shown in fig. 2(a). As soon as it detects a signal at a GPIO pin, it starts a timer which is invokes an ISR after every 156.25 microseconds (20milliseconds / 128). This ISR, running on core 0, every time it is triggered, takes six analog inputs as 'One Sample' and stores it into a buffer having a capability to store 128 samples. When this buffer is completely filled, its data is transferred to another processing buffer and sets the flag. This processing buffer is globally defined and can be used with both cores. The core 1 continuously checks for the flag and as soon as it is set, it starts the calculation of the 128 point DFT for all six analog signals (i.e. Three voltage and Three current).

The result of this calculation gives magnitude and phase angle of fundamental component of each phase voltage and current. Once the FFT of these signals is calculated, it is transmitted out of the serial port at a rate of 2Mbps. When the core 1 completes its processing it resets the flag. This process continues and multiple frames are transmitted every second.



Fig.3: Flowchart of Micro PMU Algorithm

The transmitted data frame is given to a USB-to-Serial adapter, which may be optionally used to transmit it to a Phasor Data concentrator (PDC), which is not in the scope of this work.

Fig.2 shows the arrangement of phasor measurement unit based on ESP32 development board. This board has a high computational power 32 bit microcontroller and most of the I/O pins are broken out to the pin headers on both sides for easy interfacing. The controller operates at 240MHz and has two cores which operates in parallel. A GPS receiver NEO 6Mv2 has been interfaced with the board to obtain a precise pulse per second (PPS) signal. The signals proportional to system voltage and current are interfaced with the board using ADC pins as shown in analog block. The synchrophasor frames are transmitted at 2MBPS rate to another microcontroller for transmitting it to centralised server for further processing and analysis. A LCD display is also interfaced with the controller to display the PMU frame. The display rate is selected in such a way that students can note it down and appreciate the frame sequence. The huge data generated will be available in EXCEL format for the analysis.

Result

The developed hardware has been tested in laboratory to validate the μ PMU working. The phase and magnitude of the fundamental component of voltage and current phasors are obtained by implementing the Fast Fourier Transform (FFT). The SOC and FR parameters can be accurately calculated using the GPS module and internal frequency divider technique. The generated data frame is transferred to a local server at 2MBPS rate. The sampled data frames are displayed on a LCD display using another controller for the local monitoring objective.



Fig.4: FFT of Voltage Signal

FFT analysis results for one of the voltage phase are given in fig.4.

Conclusion and Future Scope

From the prototype testing, it can be concluded that a full featured μ PMU with lower data transfer speed can be developed using a general purpose microcontroller and GPS module. The prototype can be used as novel teaching tool in the Microgrid and Smart gird laboratories and will help to demonstrate the operation of μ PMU and Synchrophasor concept. In further development, the prototype can be used for the demonstration of real time control of distributed generation sources in the laboratory.

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