
Design of Low Power CMOS Latched Comparator for Portable Medical Applications

¹C. Ashok Kumar, ²Dr. B. K. Madhavi, ³Dr. K. Lal Kishore

¹Department of ECE, Narasimha Reddy Engineering College, Secunderabad & Research Scholar, JNTU, Hyderabad

²Professor, Department of ECE, SWEC, Hyderabad, Telangana

³Professor & Dean Research, Department of ECE, CVR College of Engineering, Hyderabad, Telangana

Email:cheelikumar@gmail.com, Bkmadhavi2008@gmail.com, lalkishorek@yahoo.com

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Abstract

In this work a new architectural design of latched comparator that is suitable for implementation in portable health Monitoring applications has been proposed. In the new proposed design of the latched comparator, lower power dissipation is achieved due to the low transistor count of the circuit. Moreover the proposed comparator consists of the positive feedback mechanism to overcome the non idealities of comparator like kickback noise and offset voltage. In this paper, proposed circuit is carried out using Tanner EDA tools in CMOS technology. In this brief, work proposed is designed well to operate with the frequencies between 50 to 250 KHz and with supply voltages from 450mV to 1V. The non-idealities of the proposed comparator are considerably and power dissipation is also reduced.

Keywords

Cardiac Monitoring Applications, Low Transistor Count, Kickback Noise, Comparator

Introduction

Latched Comparators are one of the crucial components in the design of analog to digital converters (ADCs) which are very necessary in most of the applications related to signal processing. One important application is Cardiac Implantable Medical Device for monitoring cardiac Signals. Such applications are implemented in CMOS nanometer technology with a lot of digital signal processing circuits as well as analog circuits. The overall performance of the device depends on the analog to digital converter circuits. Hence, there is a need to improve comparators. These are usually energy constrained and they are battery operated. Therefore it is very essential to design the low power circuits for increasing battery life of the device [1],[2].

Cardiac Implanted Medical Device is installed with a physical contact between the tissue and the electrodes. However, it is less immune to noise sources which are outside the body when compared with the wearable cardiac medical devices. The major drawback of these systems is very expensive in cost and also requires a risky surgery. Meanwhile the lifetime of the device is very important and it is very much required to work for several years. To address this issue, our interest is on the design of a low power comparator. The vital cardiac signals are of medium speed, therefore the device doesn't need high speed but power dissipation is the major issue. A 7-bit Successive Approximation Register ADC with clock frequency as 100 KHz is used in our circuit design which is acceptable in the intended design [3, 4].

In this brief, we tried to optimize the conventional latched comparator in terms of kickback noise generated within the latch and power dissipation. Moreover we tried to optimize the comparator for frequencies between 50 to 250 KHz and between the voltages from 400mV to 1V. However, the designed latched comparator is not only used in Cardiac applications but also it can be used in other applications by simply varying the operating point.

Regenerative latched comparators or latch based sense amplifiers are used generally used in low power applications. With the existence of positive feedback mechanism, the response of the latched comparator is very fast and accurate. Moreover, low power consumption of latched comparators is due to the reduction static leakage currents [5, 6, 7, 8].

In this work, a low power based design of dynamic latched comparator architecture is presented with high resolution and accuracy. The proposed architecture of latched comparator dissipates a few Nano watts of power at medium frequency of operation. The proposed latched comparator fits into the applications where limited source energy is available. This work is organized as follows. The preceding section establishes the various architectures of latched comparators. In section III, the proposed comparator architecture is demonstrated. In Section IV, the simulation results are presented and analysed including the comparison performance of key parameters between the existing and proposed architectures of the latched comparators for cardiac IMDs. Finally in section V, conclusions are drawn.

Existing Latched Comparators in Medical Applications

Due to the existence of numerous latched regenerative comparator architectures, it is difficult to initiate the details of all the available architectures. Therefore, in this brief a few basic architectures of latched comparators are compared. In general, all the latched comparators based on the clock signal operate in two modes of operation. During the first mode or phase of operation known as reset phase, clock input is set to 0V and the input signal is given to the comparator and the positive feedback of the latch is disabled, thus both the outputs are charged to a voltage level VDD. In the second phase or mode of operation known as regeneration phase, the clock input is set to a voltage level of VDD volts and whenever the input signal is applied, the outputs reach their final values depending on positive feedback mechanism of the latch.

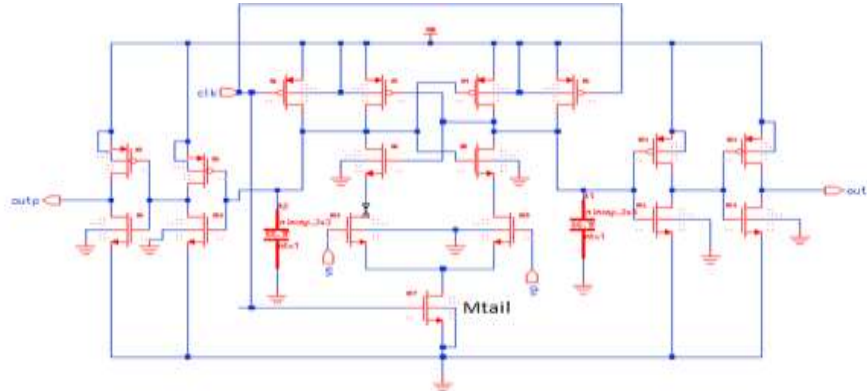


Figure 1: Schematic Diagram of Balance Latched Regenerative Comparator

The schematic of regenerative balanced latched comparator architectural design is demonstrated in figure 1[9]. In this design of the latched comparator, thermal noise is reduced to a great extent by placing the capacitors in parallel form. But reduction in thermal noise generates kickback noise which degrades the performance of the comparator. In this circuit almost all the transistors work in the weak inversion region.

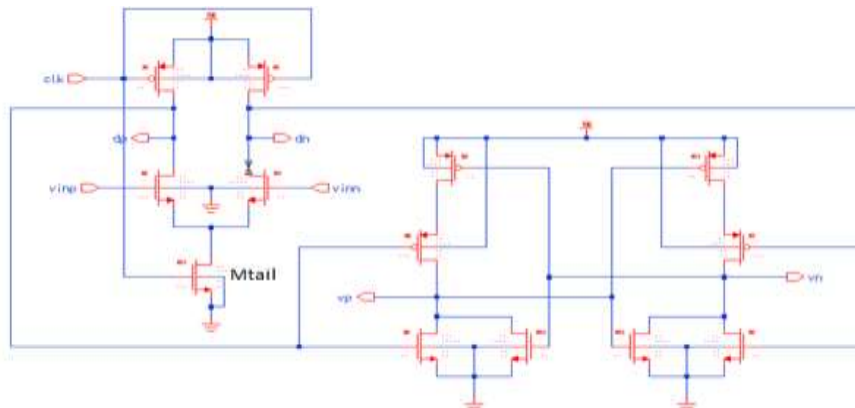


Figure 2: Schematic Representation of Dual Rail Dynamic Comparator

The architectural designed circuit of the clocked Phase dual rail dynamic comparator is demonstrated in figure 2[10]. It also works w.r.t to the applied voltage levels at the clock input. When compared with the other existing designs, this design may dissipate more power but on the other hand it generates low kickback noise. Based on the requirements, this design of comparator is implemented in the applications where less should be generated.

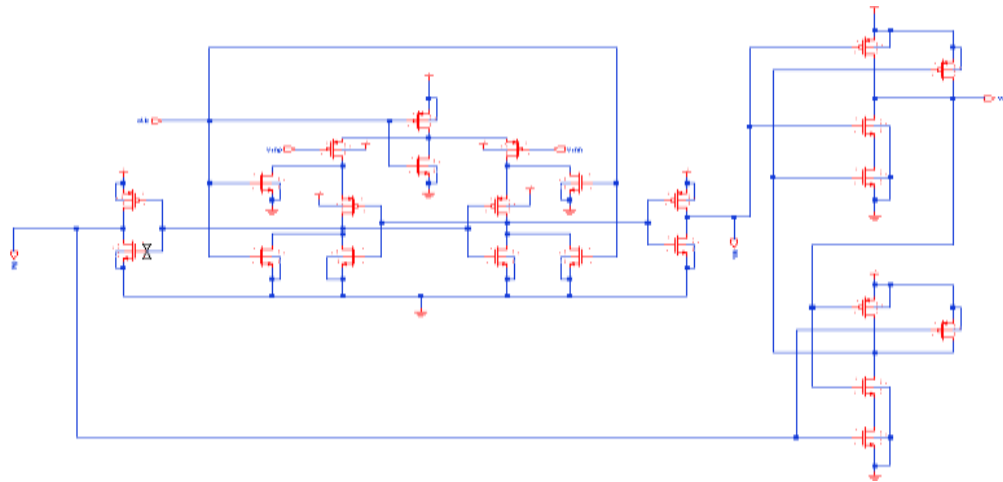


Figure 3: Schematic of SR Latched Dynamic Comparator

The schematic architecture of SR latched regenerative comparator is depicted in figure 3[11]. In this architectural design of SR latched comparator, an SR latch circuit is used in the design which is used to store the final comparison value during the regenerative or decision mode. In this circuit, with the use of two inverters loaded at the output, the comparison value is made unique. Moreover to maintain low values of thermal noise and kickback noise the input voltage is kept at mid rail voltages.

Proposed Latched Comparator

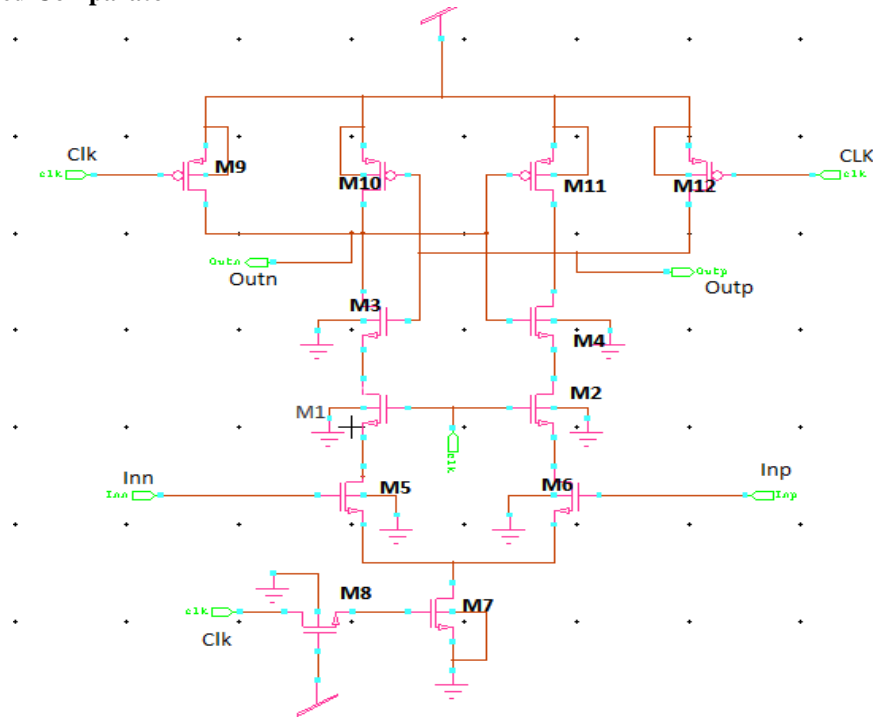


Figure 4: Proposed Architecture of Latched Comparator

In SAR ADC, the thermal noise plays a major role in degrading its accuracy. To overcome this effect the input transistors size has to be increased which are present in the latched comparator but due to this, kickback noise of the latched comparator also increases in proportional to the increase in size of the transistor. Here in this context a new latched comparator has been designed such that it overcomes the non-idealities of existing comparators such as offset voltage, thermal noise and kickback noise. For achieving low power, in this work we have chosen single stage

comparator. To address the issues of non-idealities in the latched comparators, proposed comparator uses cross coupled compensation architectural technique which is depicted in figure 4. Normally kick back occurs due to the fast transition of the voltage levels present at drains of the input transistors. In the proposed architectural design of the latched comparators, transistors M1 and M2 which are called as the compensation transistors and they are utilized in reducing the residual kickback noise.

The proposed latched comparator works in two modes of operation i.e comparison mode /phase and reset mode/phase. In the reset mode, the clock input is 0V, due to this the following transistors M9-M12 will be on ON state which intern leads the two outputs Outn and Outp to VDD which is the supply voltage for the comparator . In the comparison mode of operation, the specific transistors M1, M2-M7 will be in ON state and the transistors namely M9-M12 will be in OFF state. With the voltage levels applied at Inn and Inp one of the outputs will reach VDD and other to 0V. If voltage level at Inp is greater than voltage level at Inn, then the output Outp goes to 0V and Outn goes to VDD and vice-versa. In this proposed design, splitter footer structure and the compensation transistors are used which reduces the non-idealities of the comparator to good extent.

In this proposed architecture of latched comparator circuit, the existence of kickback noise is cancelled with the help of compensation transistors M1-M2 and these compensation transistors provides isolation at the input transistors where the input voltage has been applied. This technique will be offering shielding effect between input and output nodes of the comparator, thus decreasing the existence of kickback noise to a great extent. Also the input referred offset voltage is one of the performances metric that is used to measure the performance of the latched comparators. In the proposed architecture, the static offset voltage is kept at the mid rail voltage levels to degrade the effect of offset voltage. Based on Gaussian distribution, the proposed comparator has the offset voltage whose

deviation is $\sigma_{OS} = \Delta V_{IN_{min}} / \sqrt{2} \text{erf}^{-1}(2Y-1)$.

Simulation Results

In this brief, the proposed latched comparator is simulated in CMOS 90nm PTM technology and are analysed & presented graphically. Also the comparison of existing architectures of latched comparator is done with the proposed architecture and it is tabulated. .The Simulation is done using Tanner EDA tool.

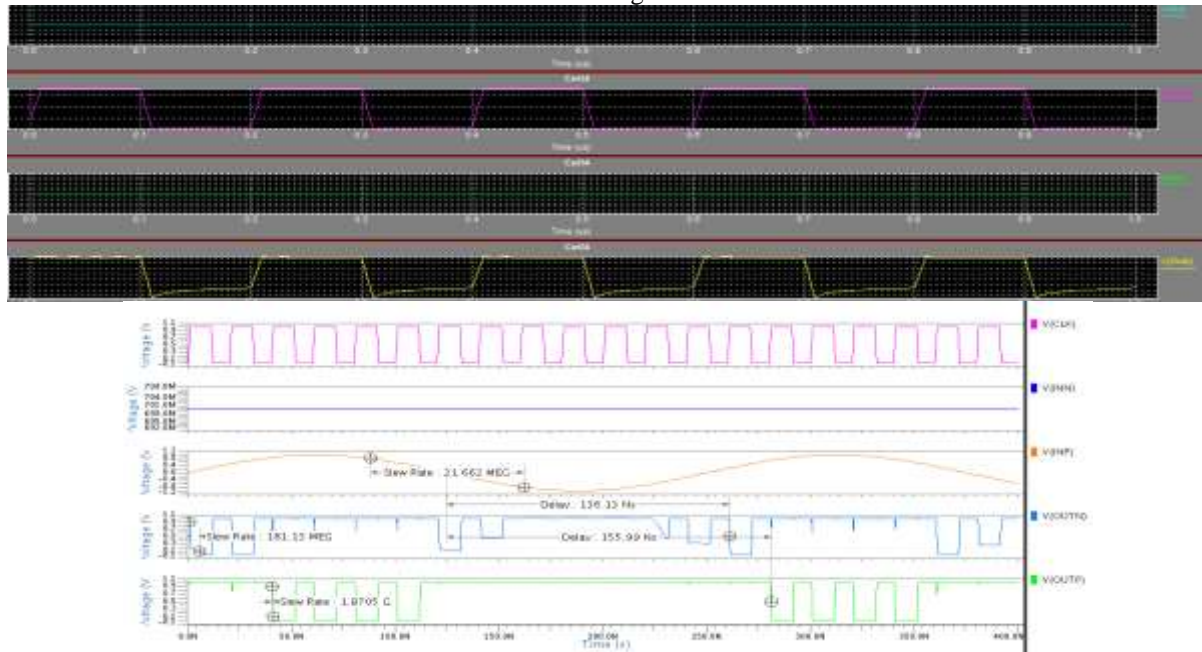


Figure 5: Transient Response of Proposed Regenerative Latched Comparator

In figure 5, with the specifications of $V_{inp}=1V$ amplitude sinusoidal wave, $V_{inn}=0.6V$ amplitude sinusoidal wave, transient response is demonstrated. The input is $Clk=1V$ with a frequency of 100KHZ.

Comparison Table I:

Comparator Properties	[11]	[10]	[9]	Proposed Comparator
Kickback Noise(uV)	580	610	1290	450
Power Dissipation(nW)	6	1.1	2.8	1.7

From the above table I, it is clear that the proposed comparator produces less kickback back noise and dissipates low power when compared with the existing architectures.

Conclusion

In this brief, various architectures of latched comparators for portable medical applications have been extensively studied and also designed a new architecture of latched comparator which is able to overcome the non-idealities of the comparator. The newly designed circuit is able achieve good considerable results and it is shown in simulation results using Tanner EDA tools. The results during the simulation of the proposed circuit shows that, the designed circuit yields low kickback noise low offset and also consumes low power when compared with other architectures used in portable medical Applications.

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