

g_m Based CMOS LNA Linearization Techniques – A Comparison

^{*1}Sumeet R. Wawarkar, ²Rupali Tawri, ³Mayank B. Thacker, ⁴Dipak Dahigaokar

^{*1,2}Department of Electronics Engineering, Shri Ramdeobaba College of Eng. and Mgmt., Nagpur

³University of Manitoba, Winnipeg, Canada

⁴Department of Electronics & Communication Engineering, Shri Ramdeobaba College of Eng. and Mgmt, Nagpur

Email: ^{*}wawarkarsr@rknc.edu, tawrir@rknc.edu, thacker5@mymanitoba.ca, dahigaonkardj@rknc.edu

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Abstract

This paper proposes g_m based CMOS LNA linearization techniques. A common source Cascode LNA with source degeneration is used as a base circuit operating on 0.8 to 2.5 GHz frequency range using TSMC 180nm technology and 1.8V supply. Linearization techniques i) Harmonic Termination, ii) Derivative Superposition, iii) complementary DS and iv) Post distortion are discussed and implemented on casode LNA. Comparison of results shows that IIP3 is improved by 17.8 dBm for Harmonic Termination, 10.7 dBm for Derivative Superposition, 8.5 dBm for Complementary DS and 20.2 dBm for Post Distortion technique.

Keywords

LNA, Linearization Techniques, Harmonic Termination, Derivative Superposition, Complementary DS, Post Distortion.

Introduction

The 21st Century communication technology has been predominantly wireless in nature and has resulted in numerous standards spanned over closely spaced frequencies governing different applications [1]. An LNA is an important block in a wireless receiver and critical for enabling robust performance in obstructed environments. The image signal is produced in the non-linear devices because of the cross terms. This image signal dominates the minimum detectable signal at the receiver of the system. In such a situation, minimum detectable signal performance cannot be improved by bringing down Noise Figure of the system. The low-noise amplifier (LNA) has to provide high linearity preventing the interfering inter-modulation tones from corrupting the carrier signal. Improve in linearity must not be at the cost of gain or NF. This requires the use of linearization techniques without much cost [1].

The organization of the paper is as follows. Section II reports the Common source Cascode LNA and its implementation. Section III discusses the linearization techniques used in this paper with the simulation results and section IV concludes the paper.

Cascode Common source LNA design:

The complete schematic of cascode LNA consisting common source stage is shown in figure 1. Common source stage is also called as the Simultaneous Noise and Input Matching (SNIM) technique, as it matches input impedance and also provides low NF for the operation of the circuit.

As shown in figure 1, transistor M1 and M2 act as LNA core. Inductances L1, L2 and capacitor C1 are utilized for broadband impedance matching. Capacitor Cg is connected to reduce the value of inductances in the matching network. Inductor Ls is used for feedback and also serves input matching.

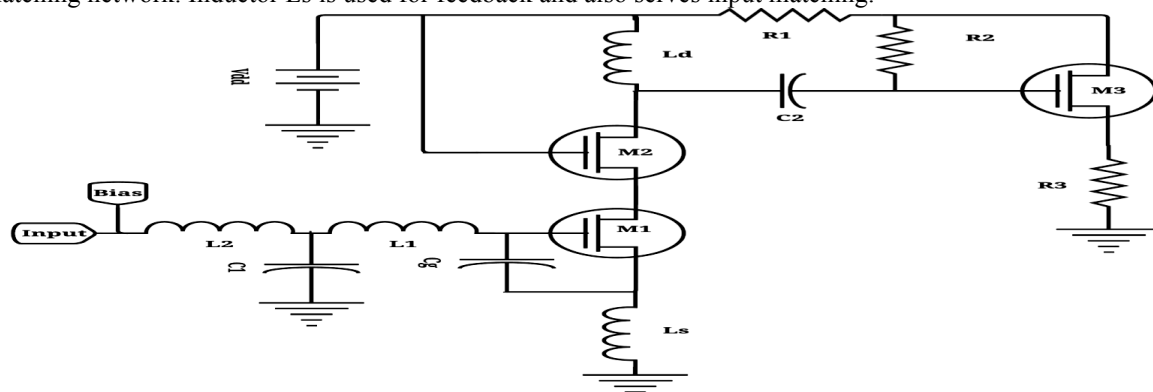


Figure 1: Complete Schematic of Cascode LNA Design with Source Degeneration

The small signal equivalent of the input side is shown in figure 1(a). The Capacitor C_{gs} has a small effect on linearity [2], we can insert an external capacitor in parallel with C_{gs} to give freedom for input transistor sizing. Biasing circuit is not shown in the schematic for simplicity.

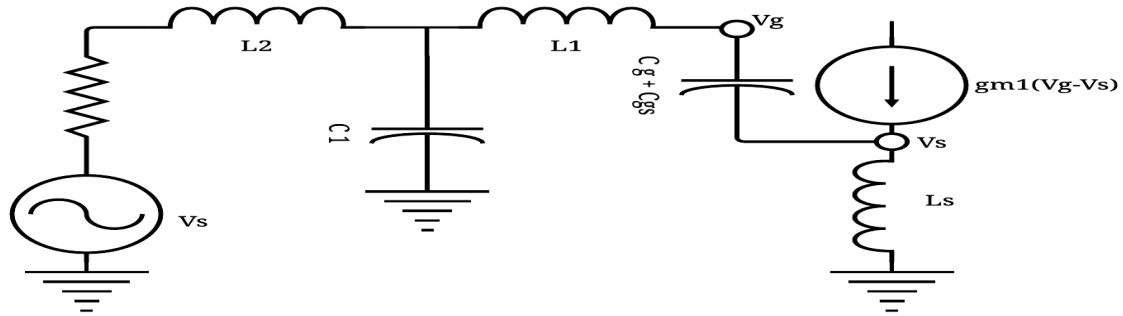


Figure 1(a): A Small Signal Model for Input Match

At resonance, the gate-to-source voltage is Q_{in} times as large as the input voltage. The overall stage transconductance (G_m) under this condition is given as [3]:

$$G_m = g_{m1}Q_{in} = \frac{g_{m1}}{\omega_0 C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega_0 R_s} \quad (1)$$

From expression, we can conclude that the overall transconductance is independent of the device transconductance. The input impedance of LNA using this circuit becomes analogous to an RLC series circuit with the extra freedom to attain greater bandwidth. This can be given by the formula [3]:

$$Z_{in} = \frac{1}{j\omega C_{gs1}} + j\omega(L_s + L_g) + \frac{g_{m1}L_s}{C_{gs1}} \quad (2)$$

Where, $C_{gs1} = C_g + C_{gs}$.

From equation (2), at the series resonance frequency of the input circuit, the inductor impedance and the capacitor impedance are cancelled out. The input impedance is then just the remaining last term in the Z_{in} equation given as:

$$Z_{in} = \frac{g_m}{C_{gs}} L_s \quad (3)$$

From equation (3), it can be seen that the impedance is proportional to source degeneration inductor L_s . The mathematical equations can be used to find optimum NFmin and Q_L at a frequency of interest for a selected value of inductor L_s . The common source Cascode LNA is simulated to perform S-Parameter and Harmonic analysis. Simulation results indicate IIP2 of 23.6 dBm and IIP3 of -4.2 dBm. NFmin is measured to be 2.7. Figure 2 shows S11 and S22 parameter analysis of the circuit. Figure 3, 4 and 5 show IIP2, NF and IIP3 simulation results respectively.

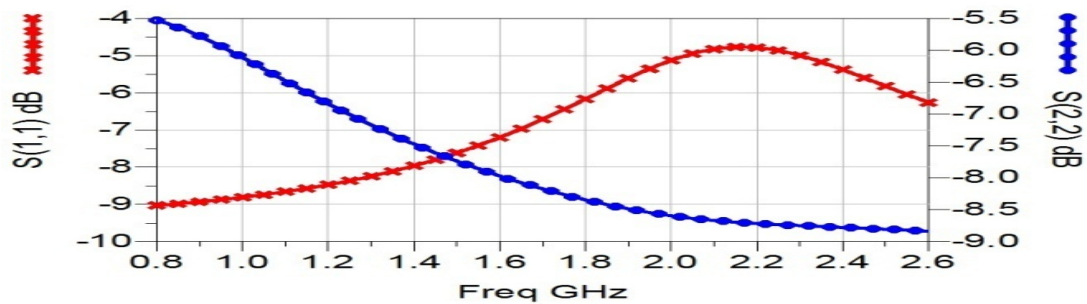


Figure 2: S11 and S22 of Cascode LNA.

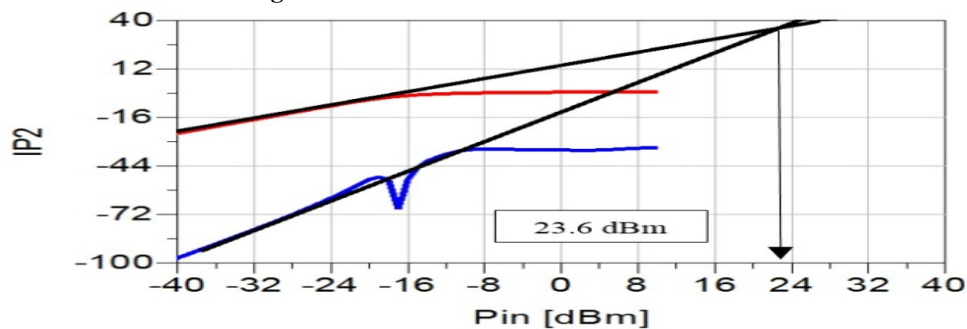


Figure 3: IIP2 of Cascode LNA

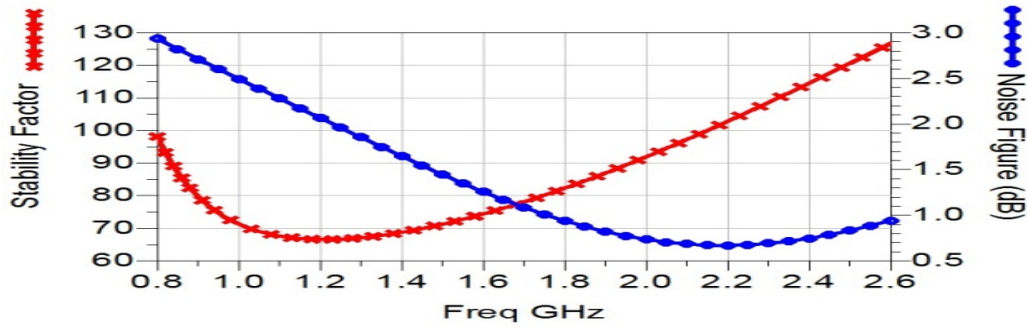


Figure 4: NF and Stability of Cascode LNA

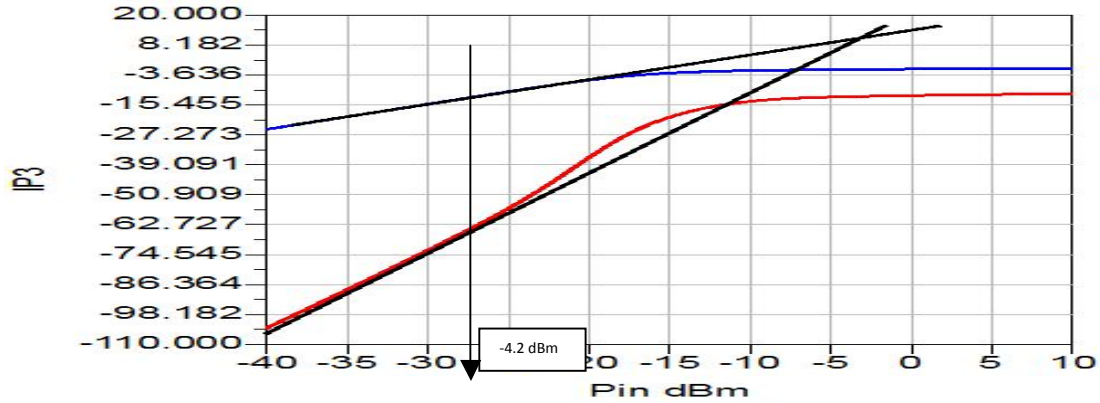


Figure 5: IIP3 of Cascode LNA

Linearization Techniques:

For improving the linearity of LNA, a number of linearization techniques have been proposed. MOSFET being a naturally linear device as compared to BJT, require high bias to realize required g_m and subsequently, linearization techniques are essential to reduce DC power [4].

Linearization techniques are fulfilled to minimize second and third order harmonic coefficients by keeping only the first, which is linear term.

For linearizing LNA, it is essential to bias the circuit near the point where MOSFET varies from sub-threshold to saturation region. Different techniques are utilized for this purpose as discussed next.

Harmonic Termination

This technique of linearization targets intrinsic third order g_m (g_3) based non-linearity. In this technique, a terminating network is added to force the corresponding node voltage to zero at the IM2 frequency [5]. An LC trap network [6] as shown in figure 6, whose frequency lies in operating frequency of LNA is used to accomplish input side termination which is harmonic of the input signal frequency.

The inductor L_h creates a high impedance at the fundamental signal frequency, so the in-band operation is not affected by the trap circuit of the amplifier. C_h capacitor is to be selected such that it will resonate with inductor L_h at the input two-tone difference frequency.

Volterra series analysis of the same circuit can be given as under [7]:

$$IIP3 = \frac{1}{6\text{Re}(Z_1(\omega) \cdot |H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\epsilon(\Delta\omega, 2\omega)|)} \quad (4)$$

Where,

Z_1 is termination impedances at frequencies $\Delta\omega$.

Z_2 is termination impedances at frequencies 2ω .

ω is the angular centre frequency of the two input tones.

$\Delta\omega$ is the two-tone frequency separation.

$$\epsilon(\Delta\omega, 2\omega) = g_3 \cdot \frac{2g_2^2}{3} [2k(\Delta\omega) + k(2\omega)] \quad (5)$$

$$H(\omega) = \frac{1+j\omega C_{gs}[Z_1(\omega) + Z_2(\omega)]}{g_1} \quad (6)$$

$$A_1(\omega) = \frac{1}{1+g_1 Z_2(\omega) + j\omega C_{gs}[Z_1(\omega) + Z_2(\omega)]} \quad (7)$$

$$k(\omega) = A_1(\omega)Z_2(\omega) \quad (8)$$

IM3 distortion is affected by the transconductance nonlinearities which can be depicted from the term $\varepsilon(\Delta\omega, 2\omega)$. From equation (5), it can be observed that the third-order nonlinearity represented by g_3 and by the second-order nonlinearity represented by g_2 generates distortion. Figure 7 and 8 show IIP2 and IIP3 simulations for Harmonic Termination. Simulation result shows significant improvement in IIP3 of 17.3 dBm. IIP2 and minimum gain are also increased. But the noise figure degrades because of the presence of passive elements in the network.

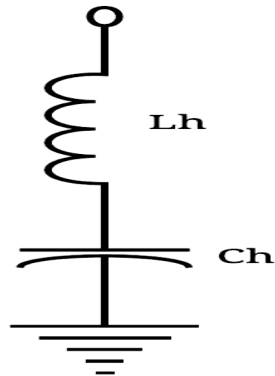


Figure 6: LC Trap Network [6]

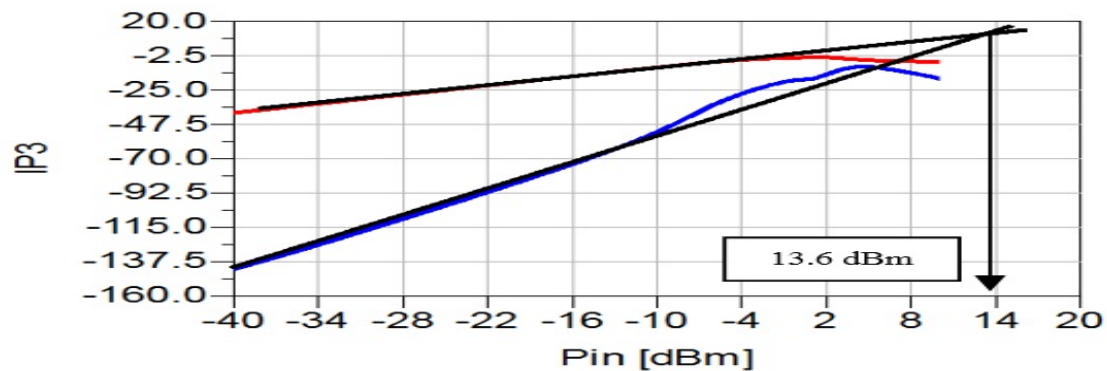


Figure 7: IIP3 for Harmonic Termination

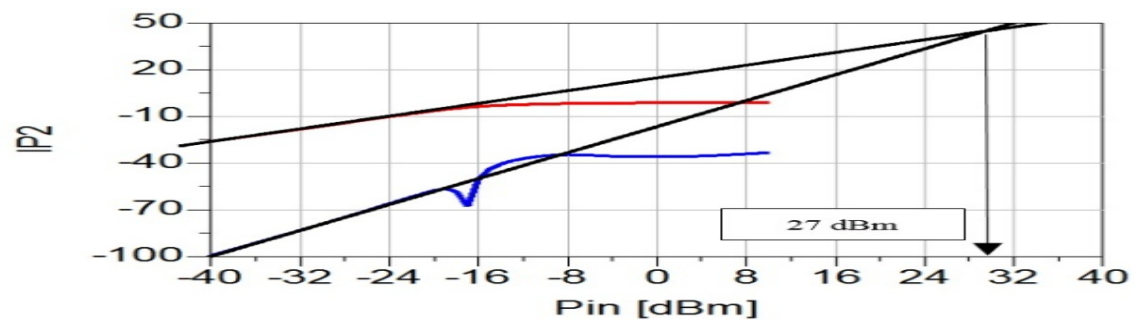


Figure 8: IIP2 for Harmonic Termination

II. Derivative Superposition (DS)

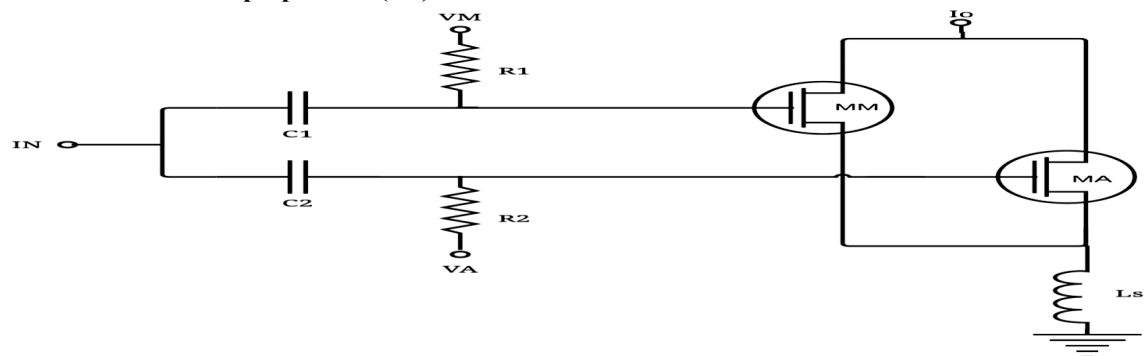


Figure 9: Schematic of DS Method [8]

By biasing MOSFET at a proper gate-source voltage (V_{GS}) we can linearize a MOSFET. At this V_{GS} voltage, the third order derivative of drain current I_D is zero. To ease the IIP3 sensitivity with respect to biasing of MOSFET, the derivative superposition (DS) technique is proposed in [8]. This technique aims intrinsic third order non-linearity (g_3). Multiple gated parallel (auxiliary) MOSFETs of different widths and gate biases are utilized by this technique. A composite DC transfer characteristic with an extended V_{GS} range in which the third order derivative is close to zero is achieved by this technique. These auxiliary transistors biased in the sub-threshold region add higher-order harmonic components because they turn on and off for large voltage swings [9].

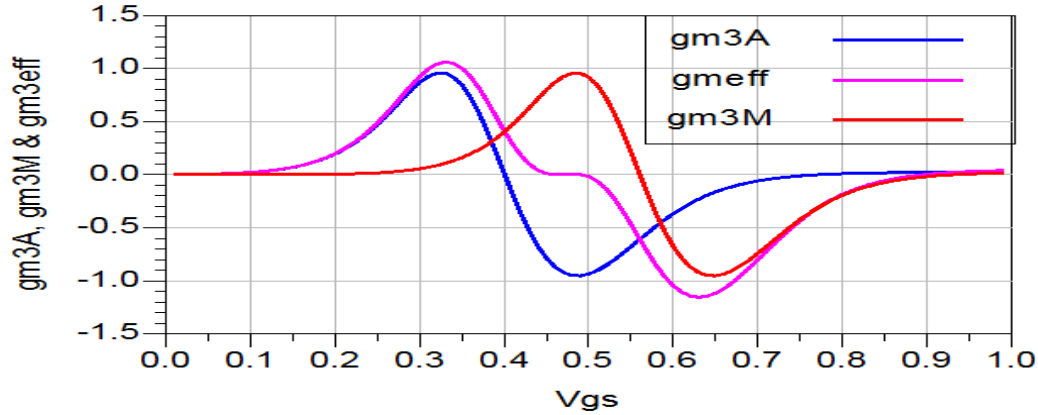


Figure 10: Effective 3 Curves Obtained in the DS Method

In Derivative Superposition, an auxiliary transistor is connected in parallel to the main amplifying transistor as shown in figure 9.

Another noteworthy property of the transistor operating in the triode region is that the curvatures of g_m for both transistors M_M and M_A oppose each other, permitting nonlinearity cancellation for large signals when the current of both transistors are combined. The effective g_3 curves are as shown in figure 10. Since transistors are connected in parallel, the system is also called as Multi gated transistor technique (MTGR). We can obtain the IIP3 equation as given in equation (9) and (10) as referred from [10].

$$IIP3 = \frac{4g_1^2\omega^2LC_{gs}}{3\epsilon} \quad (9)$$

$$\epsilon = g_3 - \frac{2g_2^2}{3} \frac{1}{g_1 + \frac{1}{j2\omega L} + j2\omega C_{gs} + \left[Z_1(2\omega) \frac{C_{gs}}{L} \right]} \quad (10)$$

As seen from equations (9), making the composite g_3 zero does not result in an infinite IIP3 as it does at low frequencies due to the second term in (10). This term represents the contribution of the second-order nonlinearity to IMD3. As expected, this contribution depends on the degeneration inductance. This result indicates that IIP3 dependants on the total g_m , g_{m3} and total g_{m2} . Other variables including the source degeneration inductor, C_{gs} , and the input impedance affects IIP3. The size and bias point of the additional transistor should be chosen considering the above parameters.

Only a small amount of additional current is required since the additional transistor is operating in the sub-threshold region. Hence, this method can improve IIP3 without any significant power overhead.

A significant design consideration in this scheme is that the delays from the main circuit path and the auxiliary paths must be identical at RF frequencies so that the nonlinearity cancellation is carried out with adequate accuracy at the required frequency range [11]. Frequency response such as, S21 and Noise Figure degrades because there is an increase in the input parasitic capacitance by at least 70%. The bandwidth of LNA also significantly reduces. These drawbacks are unavoidable, as the additional transistor size should be similar to that of the main transistor [12]. Figure 11 and 12 show simulation results for IIP2 and IIP3. The IIP3 is improved by 10.7 dBm which is less than the Harmonic Termination technique but noise figure degradation is slightly smaller. Minimum gain and IIP2 improvement are also observed here.

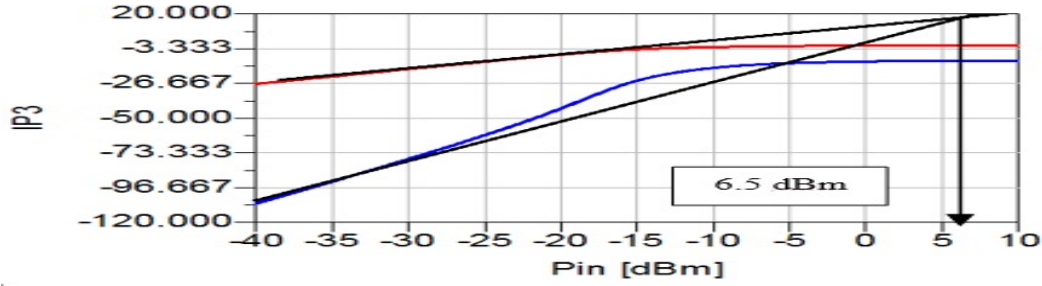


Figure 11: IIP3 for DS

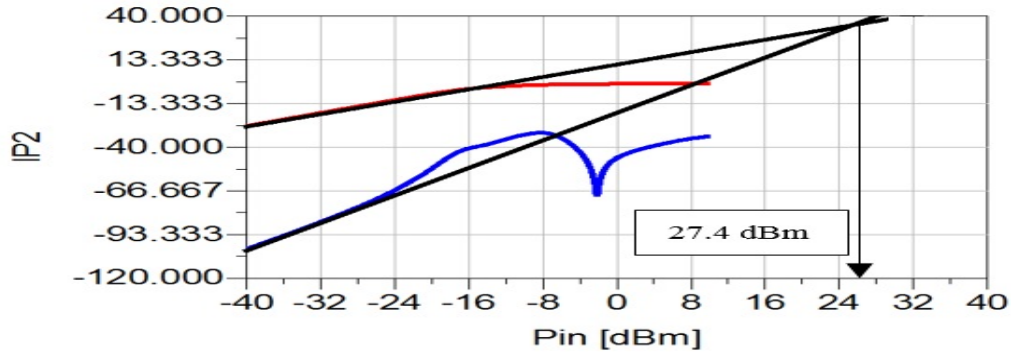


Figure 12: IIP2 for DS

III. Complementary DS

This method targets intrinsic second (g_2) and third order (g_3) nonlinearities of MOSFET. An additional P-MOS is connected to the main device whose region of operation is similar to the main N-MOS.

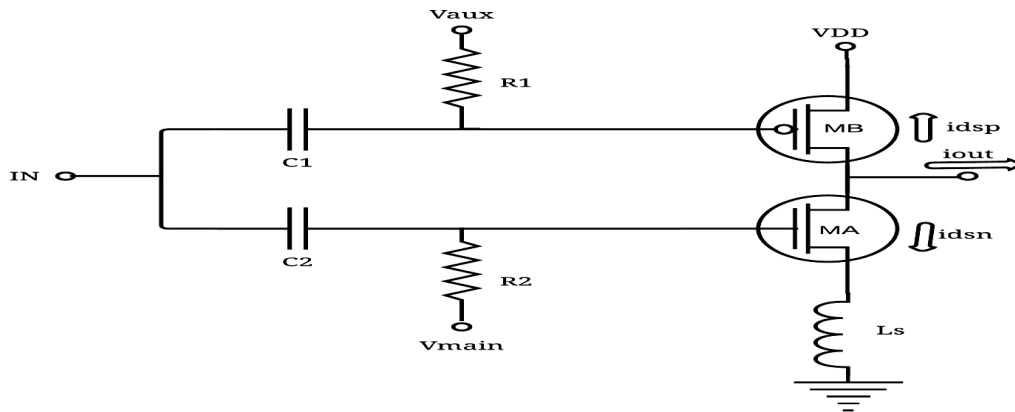


Figure 13: Schematic of Complementary DS Method [5].

Opposite currents flow from both devices which operate as an inverter amplifier and driving to effective improvement of IIP2 as well as IIP3. To fully utilize the RF performance of NMOS and PMOS in a complementary fashion while holding the thermal noise cancelling, complementary components consisting of transistors are added to the existing configuration [13]. The schematic of this technique is shown in figure 13. An added degree of freedom is obtained as g_{m3} cancellation window obtained is higher in complementary DS as compared to conventional DS method. In the circuit since the ac input signal for N and P MOSFET are out of phase, the output current is given as [5].

$$i_{dsn} = g_{1A}V_{gs} + g_{2A}V_{gs}^2 + g_{3A}V_{gs}^3 \quad (11)$$

$$i_{dsp} = -g_{1B}V_{gs} + g_{2B}V_{gs}^2 - g_{3B}V_{gs}^3 \quad (12)$$

From the circuit topology, we can infer that

$$i_{out} = i_{dsn} - i_{dsp} = (g_{1A} + g_{1B})V_{gs} + (g_{2A} - g_{2B})V_{gs}^2 + (g_{3A} + g_{3B})V_{gs}^3 \quad (13)$$

From the equation, it is obvious that total g_m increases, as g_{2A} and g_{2B} have same sign resulting in a decrease in IM2. IM3 also reduces due to same signs of g_{3A} and g_{3B} . IM2 is shown graphically along with output current in figure 16.

IIP3 enhancement is restricted at higher frequencies due to second order interaction once the third order interaction is cancelled by DS technique [12]. Figure 14 and 15 shows simulation results for IIP2 and IIP3. 8.2 dBm of IIP3 improvement is noted in this technique. Minimum gain is increased and maximum gain is nearly unchanged. IIP2 improvement is higher than Harmonic Termination and Derivative Superposition method. Noise Figure degradation is observed.

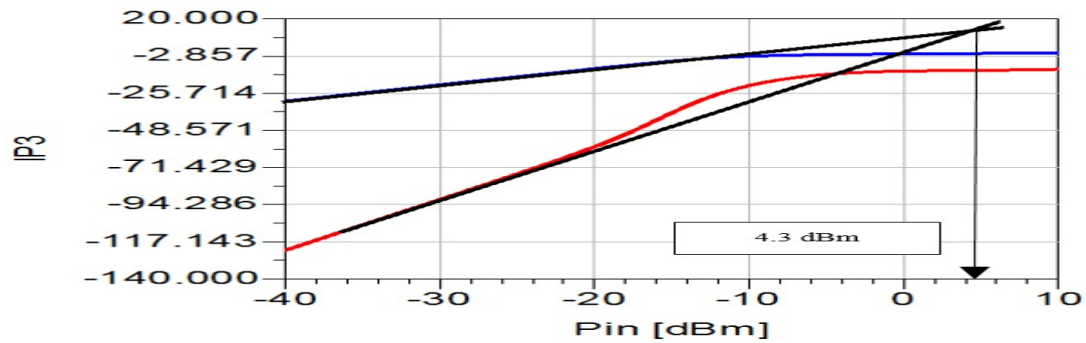


Figure 14: IIP3 for Complementary DS

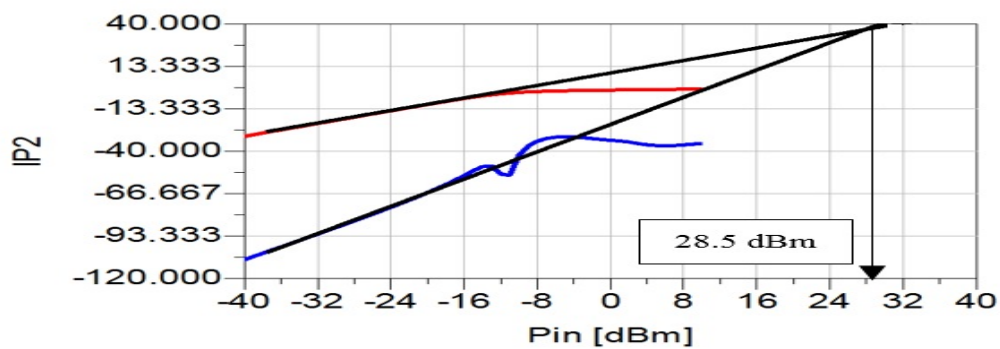


Figure 15: IIP2 for Complementary DS

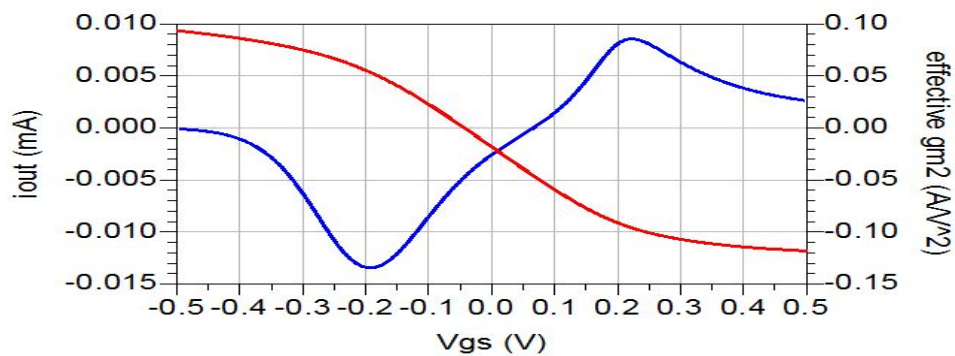


Figure 16: Output Current and Effective gm_2 of Complementary DS

IV. Post Distortion

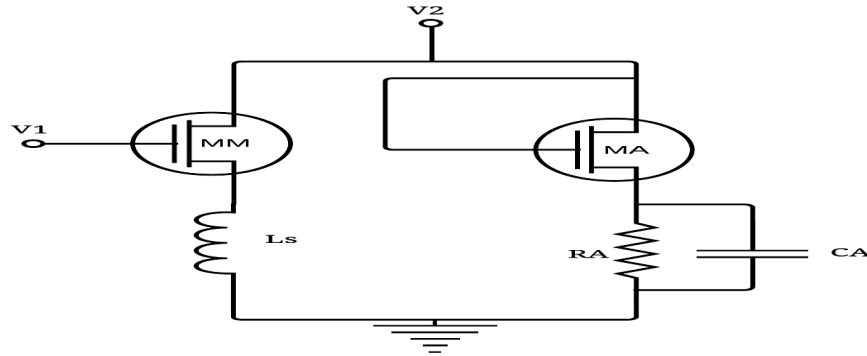


Figure 17: Post Distortion Technique [14]

This technique targets intrinsic second order (g_2) and third order non-linearity (g_3). As in DS technique, this technique too uses an auxiliary MOSFET to cancel nonlinearity that of the main MOSFET but has two main differences as [5]:

1. Auxiliary MOSFET is not connected as a parallel device, thus input side matching concerns are removed.
2. Auxiliary MOSFET work in the saturation region, making robust distortion cancellation. Schematic for the same technique is as shown in figure 17.

Transistor M_A is included to introduce additional degrees of freedom, and for linearity optimization. Resistance R_A and capacitor C_A form an intermodulation sinker along with auxiliary MOSFET M_A . M_M is the main amplifying MOSFET. Capacitor C_A actually serves for AC grounding of the signal. R_A along with Diode connected MOS generates intermodulation terms. For the linear circuit, the optimum value of R_A and MOSFET aspect ratio are selected. R_A is actually used to control the drop across diode-connected MOSFET [14]. Diode-connected transistor M_A linearizes the current. From figure 17, the v_2 voltage is tapped by auxiliary transistor M_A replicating the nonlinear drain current of the main transistor, partially cancelling both second- and third-order distortion terms. The nonlinear drain currents of transistor M_M and M_A can be expressed as [5]:

$$i_M = g_m V_1 + g_2 V_1^2 + g_3 V_1^3 \quad (14)$$

$$i_A = g_{mA} V_2 + g_{2A} V_2^2 + g_{3A} V_2^3 \quad (15)$$

Next, suppose v_2 is related to v_1 by

$$V_2 = -b_1 V_1 - b_2 V_1^2 - b_3 V_1^3 \quad (16)$$

Where b_{123} are in general frequency dependent terms and can be extracted from the simulation. The output current i_2 is given by adding the two nonlinear current i_M and i_A at node v_2 as shown in equation (17):

$$\begin{aligned} i_2 = i_M + i_A = & (g_m + b_1 g_{mA}) V_1 \\ & + (g_2 - b_1^2 g_{2A} - b_2 g_{mA}) V_1^2 \\ & + (g_3 - b_1^3 g_{3A} - b_3 g_{mA} - 2g_{2A} b_1 b_2) V_1^3 \end{aligned} \quad (17)$$

The third term in equation (17) which is the 3rd order distortion of the output current should be close to zero. This is to get good IIP3. However, the linear term is partially cancelled by transistor M_A but the gain/NF is not significantly degraded by it because its biasing is lesser than M_M . Finally, it must be noted that to improve matching and hence the cancellation of harmonics, M_M and M_A uses identical finger sizes [15]. Figure 18 and 19 show IIP2 and IIP3 simulation results of Post Distortion. This technique shows significant improvement of 20.2 dBm in IIP3 than previously discussed techniques. Noise Figure degrades by only 0.3. Maximum gain is reduced but the minimum gain is improved slightly.

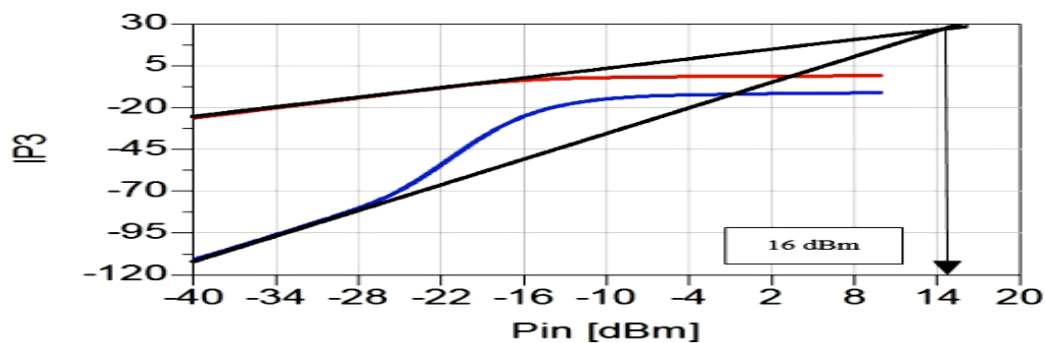


Figure 18: IIP3 for Post Distortion

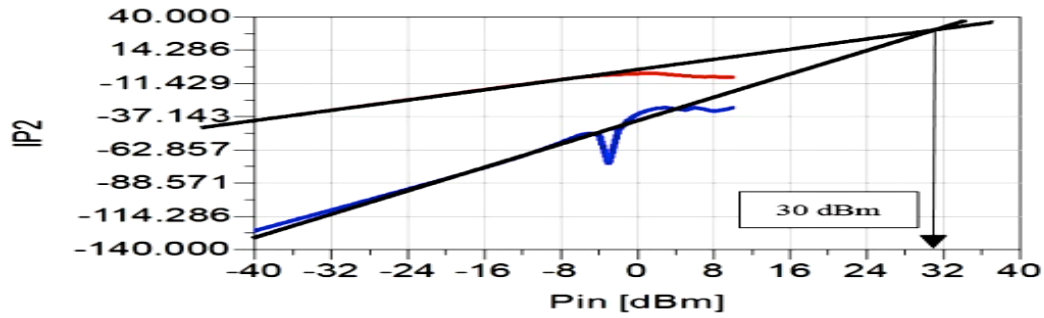


Figure 19: IIP2 for Post Distortion

Conclusion

In this paper, a comparison of different gm based LNA linearization techniques along with simulation results has been presented. The conventional Inductive source degeneration cascode common source LNA does not provide a significant linearity at RF frequency. Linearization techniques are applied to the cascode circuit and significant improvement of linearity is observed. HB analysis when performed at different frequencies having equal powers and close frequency spacing, gives largest inter-modulations. The measured results with applied linearization techniques show that the techniques can improve linearity performance with small Noise Figure and little gain loss. When the results are examined, it is seen, post distortion method has a slight increase in noise figure than the other methods and it is highest increase in Harmonic Termination technique. A relatively good gain is seen in Derivative superposition technique. Minimum gain is nearly same for all other three techniques which is around 13.5 dB.

Linearization Technique	Source (IEEE)	Maximum gain (dB)	NF min (dB)	IIP3 (dBm)	Frequency range (GHz)	CMOS Tech. (nm)
	Cascode LNA	12 - 18	2.7	-4.2	0.8-2.5	180
Harmonic Termination	[16]	20.4*	1.92	-4.4	2.2	350
	[17]	15.7*	1.4	11.7	0.88	500
	This work	13.5 – 15.8	5.6	13.6	0.8-2.5	180
Derivative Superposition	[18]	12.5*	4.5	-4	0.47-0.86	180
	[19]	9.75*	3	-2.5	0.05-0.86	180
	[20]	15.3*	2.9	2.7	2.2	250
	This work	14 - 16.5	3.3	6.5	0.8-2.5	180
Complementary Derivative Superposition	[21]	14*	3	3	0.048-1.2	180
	[22]	13.7*	2	0	0.002-1.6	250
	[23]	12*	2.6	16	0.1-1.6	130
	This work	13.5 – 17.5	3.4	4.3	0.8-2.5	180
Post Distortion	[24]	16.2*	1.2	8	0.869-0.894	250
	[25]	12.8*	1.4	13.3	2	180
	[26]	12.5*	2.7	16	0.8-2.1	130
	This work	13.3-15.2	3	16	0.8-2.5	180

*maximum gain

Table1: Performance Comparison

It is observed that in Table 1, IIP3 value of the post distortion are is much better than the other techniques used which is 16 dBm. Second highest increase in IIP3 is observed in Harmonic termination method and followed by Derivative Superposition and Complementary Derivative Superposition Technique. Complementary Derivative method has given lowest improvement in IIP3 of 8.5 dBm. Among these four techniques, Post Distortion technique is best option to boost linearity of LNA.

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