

Performance Analysis of N-Type Gated Diode Three-Transistor DRAM in 180nm Technology

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Abstract

In this paper three-transistor n-type gated diode DRAM cells have been designed and analyzed. In this design storing capacitor is replaced by n-type gated diode to improve memory read/write operation. In today's world to store digital data, demand of semiconductor memory increases day by day. Generally in embedded DRAM, SRAM is widely used because of its high speed of operation, high noise margin and good logical compatibility. But, SRAM cell consists of six transistors; hence its cell area gets increases and also consumes more power. So, a novel solution has been proposed in this paper to replace capacitor in DRAM by n-type gated diode. Design of 3T-1D DRAM cell is compared with different input voltages and different technologies to calculate power dissipation.

Keywords

Power Dissipation, SRAM, DRAM, Gated Diode

Introduction

Day by day, world demand for large data storage capacity chips in small size. Hence the design becomes scale down day by day. In most of hand held devices consist of SRAM as a memory storage device because of its high speed of operation. This memory is further divided into volatile and non-volatile memory. Non-volatile memory is further classified into read only memory, magneto-resistive random access memory and flash memory. Volatile memory is further classified as static memory and dynamic memory. The SRAM consist of latch hence data was retained as long as power is turned on whereas DRAM cell consists of capacitor to store binary information and transistor to access this capacitor.

This capacitor either charged or discharge. When it charge is stored the value '1' and when discharge it retained the value '0'. The usage of a capacitor as a primary storage device generally enables the DRAM cell to be realized in a much smaller silicon area compared to the typical SRAM cell [2]. DRAM with capacitor was not suitable for VLSI design because fabrication of capacitor was critical job. Also capacitor shows leakage current and hence periodic refresh was required. So this proposed work replaces capacitor with the help of diode. Generally read/write operation performed by RAM. Hence with the help of proposed work i.e. three transistor and one diode it will be possible to perform all operations of RAM.

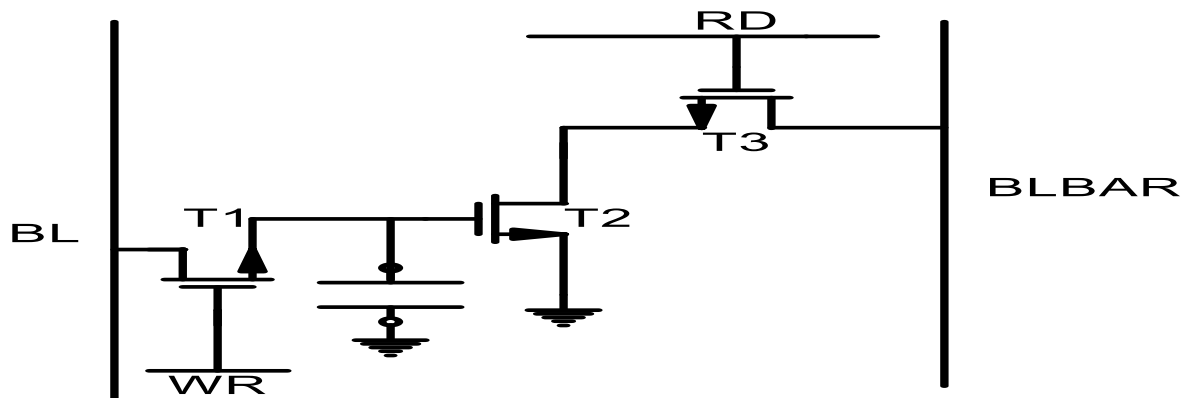


Figure 1: 3T-1C Cell DRAM

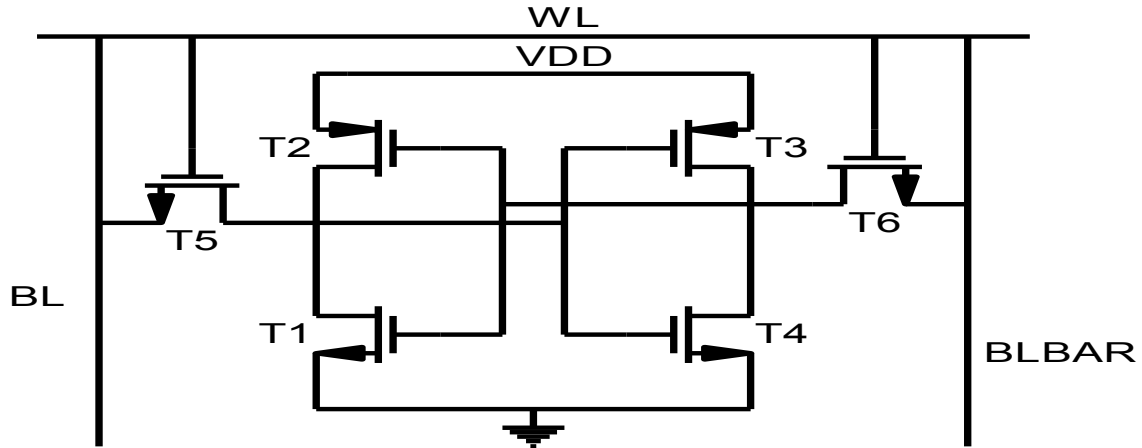


Figure 2: 6T SRAM Cell

Proposed DRAM Cell with 3T-1D

The proposed 3 Transistor- 1 Diode cell shows schematic view of basic cell of array in DRAM. In this capacitorless DRAM the charge placed on storage node S, when transistor T1 is activated and BL written write the data on it. This capacitorless DRAM gives non destructive read process. Also number of transistor required for DRAM cell is minimum as compared to 6-T SRAM cell. Hence it implies more compact cell structure as compared to SRAM. If we have to write the cell at the BL write line level, it is only required to activate T1 through the WL write line. Hence, the storage node S stores either 0 or $V_{dd}-V_{th}$ voltage depending on the logic value. This voltage results in the accumulation of charge at the gate of devices D and T2 [1].

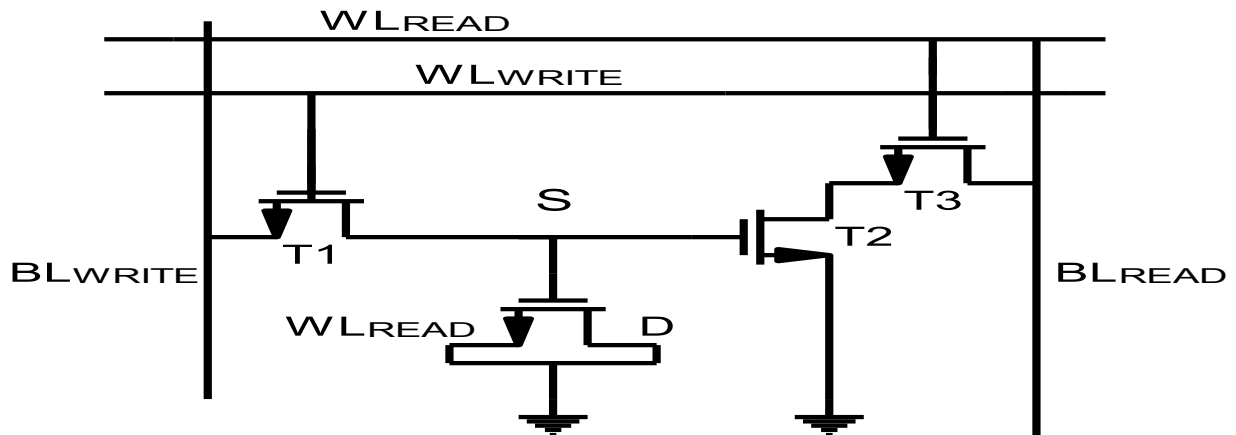


Figure 3: 3T-1D DRAM Cell

Operation of 3T-1D Cell:

The schematic view of 3T-1D cell in $1\mu\text{m}$ technology is shown below. In order to write the data to the cell, the write bitline is charged to that value we wish to store in the cell, and the write word line is strobe. Similarly, in order to write to the cell, the write bitline is charged to the value we wish to store in the cell, and the write wordline is strobe. To read from the cell, the read bitline is precharged high and the read wordline is strobe.

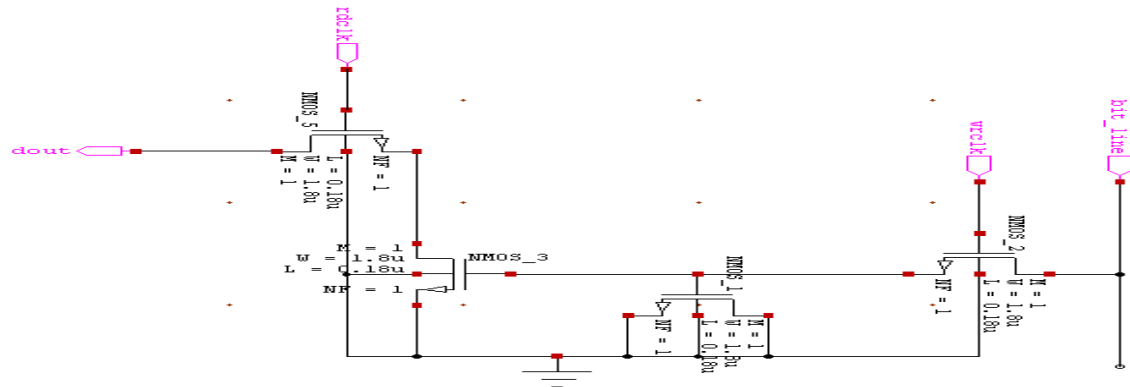


Figure 4: Schematic of 3 Transistors –1 diode DRAM Cell

In this 3T-1D cell to write data on storage node we have to raise wrclk high and hold rdclk low, then data are written on storage node S from bit_line through T1 by considering 0V for 0-data and high for 1-data. Similarly, for reading bit_line is previously precharged to high and rdclk is getting trigger from GND to high. For read 1, the capacitance on storage node S i.e. Cgs is large as the channel is on and hence the node voltage (V-storage) is boosted high and transistor T2 on strongly. After that the voltage at bit_line is discharge through transistor T3, T2 and GND. During read 1, the storage node i.e. gated diode boosted the voltage on storage node and read operation become faster as compare to 3T-1C cell hence, result of it in 3T-1D DRAM read access time is get reduced. Similarly, for read 0, cgs is much smaller because channel is off and hence voltage on storage node 0 and at that time T2 remain in off state. The input and output of 3T-1D DRAM cell in 0.18 μm Tanner technology is shown below.

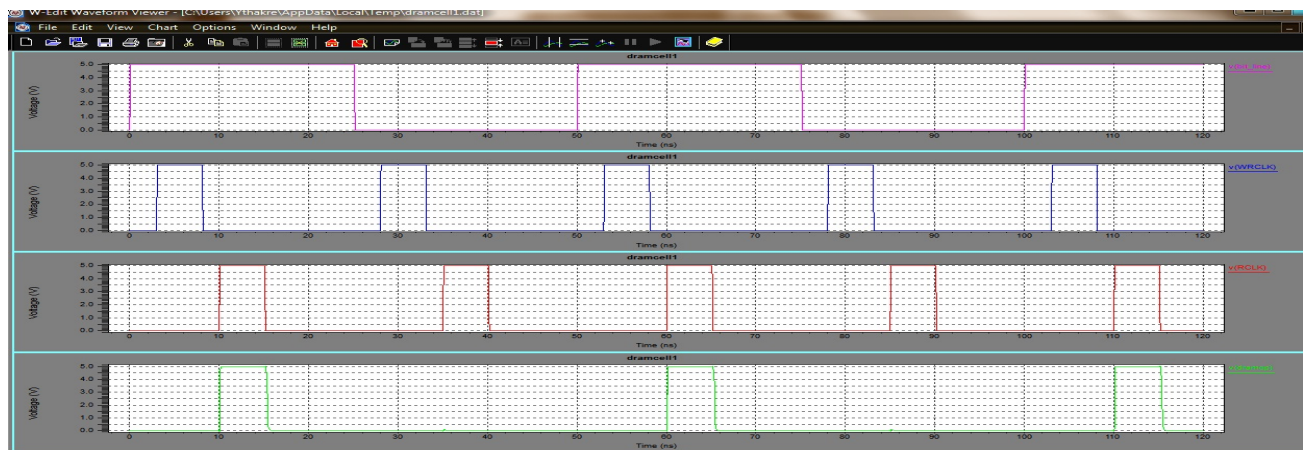


Figure 5: Input / Output Waveform of 3 Transistors - 1 Diode DRAM Cell

Proposed 4x4 DRAM Cache Architecture:

In the proposed 4x4 (16 bit) 3T-1D DRAM architecture consists of 3T-1D cell as basic building block (cell) as shown in figure 6.

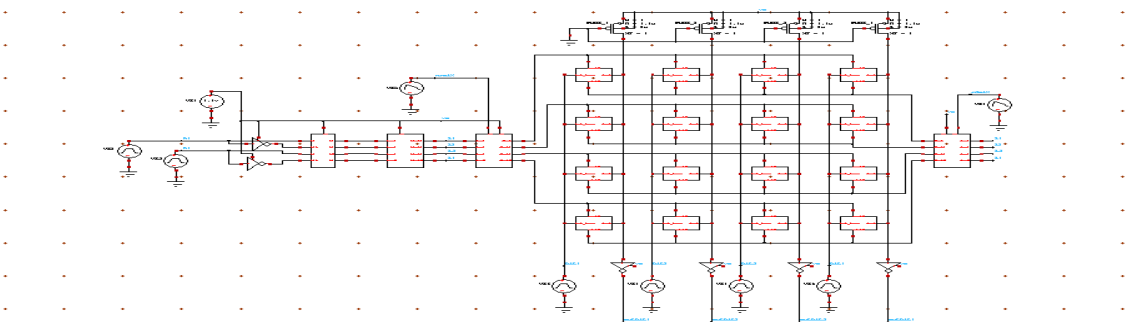


Figure 6: Proposed 4x4 (16 Bit) 3T-1D DRAM

The 4x4 3T-1D DRAM has consists of bit_line, outbit_line and also two control signals such as wr_clk and rd_clk .

A) *Bit_line*: It is input source bit for DRAM.

B) *Wr_clk*: To write a data into the cell, write word line *Wr_clk* is made high which turns ON the particular transistor. Then write bit line WBL is also made high. The data is stored in the diode.

C) *Idle*: In idle case all the signals are turned OFF.

D) *Storage Node*: The data stored in the diode can retained by enabling control line high by using Pull up PMOS network.

E) *Rd_clk*: To read the stored data from the cell, rd_clk is made high and stored data is passing on particular out_line.

F) *Outbit_line*: The stored data from memory is come out on outbit_line.

The simulated output of 4x4 3T-1D DRAM is shown below in figure7.

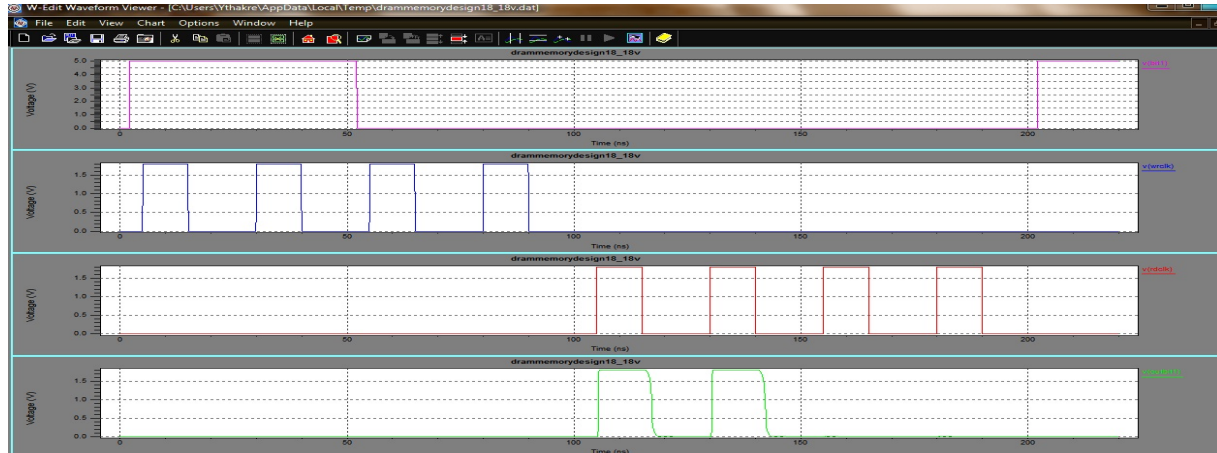


Figure 7: Output Waveform of 4x4 3T-1D DRAM

Performance Analysis:

For performing and analyzing 4x4 DRAM, Tanner-13 EDA tool is used. Two analyzing methods are generally used to calculate power dissipation in DRAM. The first method is by computational analysis in which voltage is kept constant and technology parameter is changed. In second method the technology parameter is kept constant and voltage is varied.

A) Computational Analysis

In this method voltage is kept constant and technology get changes for same DRAM architecture.

1. Voltage constant at 1.8 V

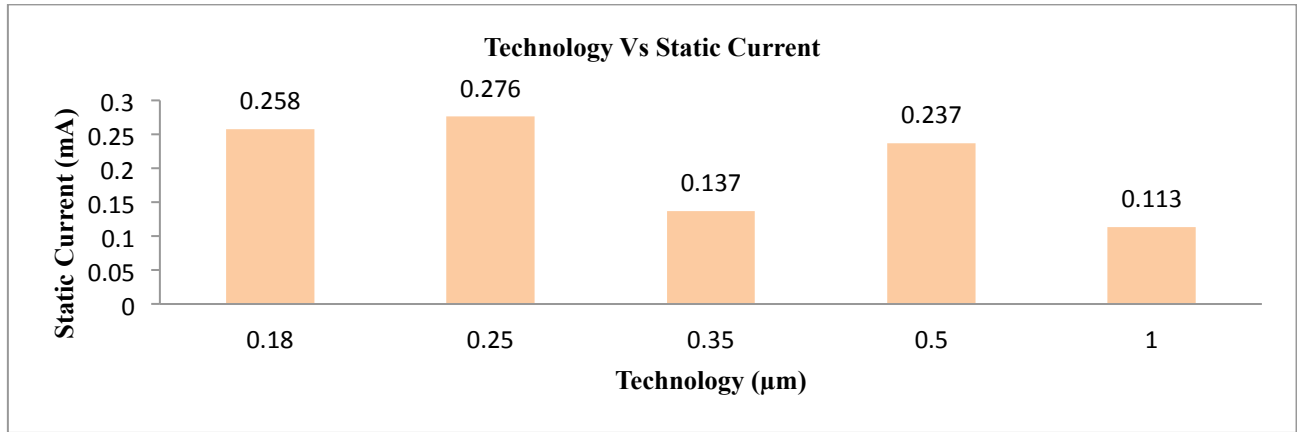
In this method of analysis applied voltage to DRAM is kept constant at 1.8V and technology parameter is varying from 0.18 μm to 1 μm . As technology parameter change, power dissipation calculated by T-spice command also shows different value. The table 1 shows power dissipation at different technology versus constant input voltage.

The static power in DRAM is given by;

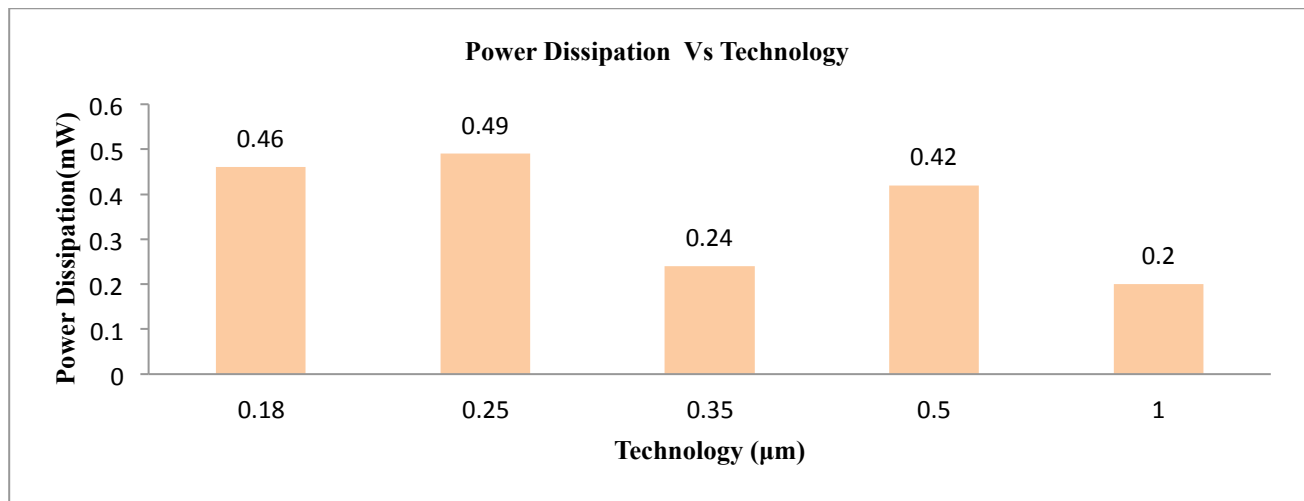
$$\text{Static Power/Dissipated Power} = VDD * I_{\text{Leakage}}$$

Technology (μm)	Static Current (A)	Power Dissipation (mW)
0.18	2.58×10^{-4}	0.46
0.25	2.76×10^{-4}	0.49
0.35	1.37×10^{-4}	0.24
0.5	2.37×10^{-4}	0.42
1	1.13×10^{-4}	0.20

Table 1: Power Dissipation in 3T-1D DRAM at 1.8V



Graph 1: Technology Vs Static Current



Graph 2: Technology Vs Power Dissipation at 1.8V

From the above graph it is clear that when applying voltage 1.8V, at that time we get minimum power dissipation at 1 μm .

2. Analytical Analysis

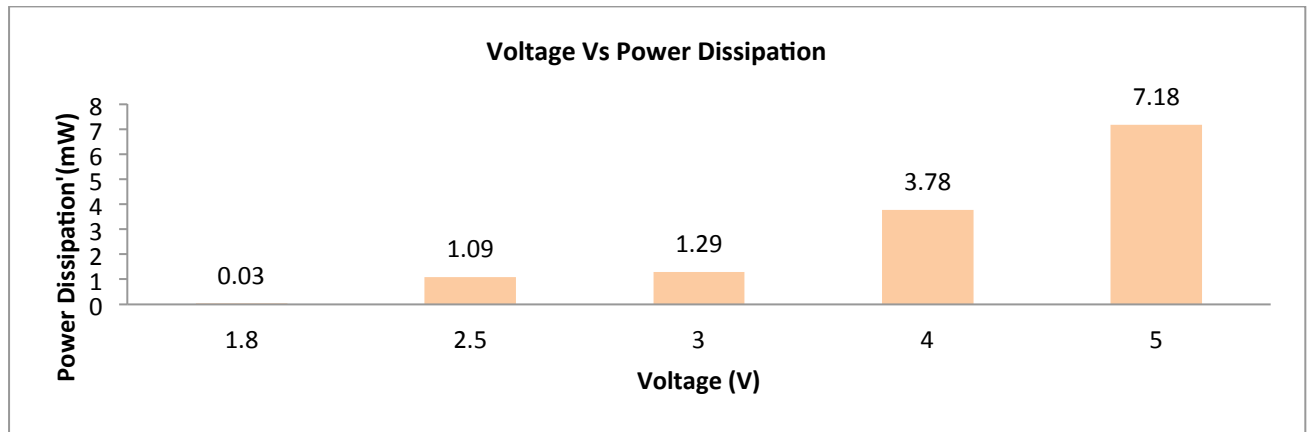
In analytical analysis technology parameter is kept constant and voltage ranges from 5V, 4V, 3V, 2.5V and 1.8V.

2.1 Technology constant 0.18 μm

In this case technology is kept constant i.e. 0.18 μm and applying voltages changes from 5V, 4V, 3V, 2.5V and 1.8V for same 4x4 3T-1D DRAM architecture then we get different power dissipation for different voltages. The leakage current and power dissipation for different technology is shown below.

Voltage (V)	Power Dissipation (mW)
1.8	0.03
2.5	1.09
3	1.29
4	3.78
5	7.18

Table 2: Power Dissipation at 0.18 μm Technology



Graph 3: Voltage Vs Power Dissipation at 0.18 μm Technology

From the above graph it is clear that when technology is constant and voltage is varied then we get minimum power dissipation at 1.8V.

Conclusion

The DRAM Cells have many advantages as compared to SRAM Cells. The 3T-1D DRAM cell performance is analyzed at different voltage levels and at different technology parameters using Tanner EDA tool. In comparative analysis of 3T-1D DRAM, it is observed that as the technology parameter and input voltage decreases, the power dissipation also goes down. Further research can be carried out to get high stability, reduce retention time and the ability to tolerate performance variation. This approach provides a comprehensive solution to many of the issues that will impact on-chip memory design in nano scale process technologies.

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