

## Design of Carry Skip Adder using Concatenation and Incrementation Scheme

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### Abstract

In Today's digital world biggest challenge is to reduce delay for increasing speed and efficiency of digital devices. In carry skip adder to achieve high speed we need to lower the path delay. Where, the carry generated should be driven to the output as fast as possible, thereby in results reduces the worst path delay which determines the ultimate corresponding speed of the digital structure. In Conventional Carry Skip Adder (Conv-CSKA), the speed enhancement parameter can be achieved by using concatenation and incrementation schemes. In this paper to achieve high speed, multiplexer logic in Conventional CSKA structure is replaced by AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) compound gates.

**Keywords:** Carry Skip Adder, Path Delay, Conventional Carry Skip Adder (Conv-CSKA), AND-OR-INVERT (AOI), OR-AND-INVERT (OAI).

### Introduction

Adders are necessary and one of the most extensively used component in the digital integrated circuit design. Adder is key building block in Arithmetic and Logical Unit (ALU) and play a major role not only in addition operation but also in multiplication, subtraction operation. Speed, Power Dissipation, Area, Delay and Energy consumption these are vital points taken into consideration while designing any adder and it strongly affect the performance of processors. The carry skip adder (CSKA) is the adder which has area optimized structure that has greater speed with lower energy requirement. In carry skip adder time required to propagate the carry is reduced by skipping over a group of consecutive stages of adder. To reduce critical path delay of adder the standard carry generates propagate logic is used and for less power consumption ripple carry blocks are used. The delay can be balanced by using the 'generate propagate' logic along with the number of inputs to the skip logic which limits the critical path delay.

There are number of different adder's family available in digital world and they are categorized by their respective different parameters like delays, energy consumption, power consumption, area usage and number of transistors. Examples of

different adder's families are Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Carry Increment Adder (CIA), Carry Skip Adder (CSKA) and Parallel Prefix Adders (PPAs). The Ripple Carry adder (RCA) is a simple adder which has simple design structure with lowest area and less power consumption but with one drawback of worst critical path delay. In Carry Select Adder (CSLA) some parameters like area required, speed and power are significantly larger than those of the RCA parameters. In case of Parallel Prefix adders (PPAs) which is also named as Carry Look-Ahead Adders, exploits direct parallel prefix structures to produce the carry as fast as conceivable. In Parallel Prefix adders there are number of altered types of parallel prefix algorithms with different performances. It should be noted that if we compare other adder's family with PPAs then the structure complexity of PPAs is higher than others adder's family.

In all adder's families the Carry Skip Adder is an efficient adder in case of power consumption and area requirement. If we compare RCA with CSKA then, CSKA has much smaller critical path delay but area and power consumption are same as RCA. This project mainly focuses on delay reduction by modifying conventional structure of CSKA and it contributes spectacular features of carry skip adder. The modified Proposed Carry Skip Adder (CI-CSKA) is design using some gate level modification and replacement in conventional CSKA for enhancing speed and power reduction of adder in result with high performance and efficiency. The aim of this project is to Implement Conventional Carry Skip Adder (CSKA) and modified proposed Carry Skip Adder (CI-CSKA) using Cadence virtuoso tool and to compare both adders simulation result in terms of delay and power.

### Carry Skip Adder

Carry Skip Adder is a structure form by using simple ripple carry adder for adder Implementation and distinct speed up carry chain called skip chain. Carry Skip Adder is a proficient adder in terms of delay, power consumption and area requirement.

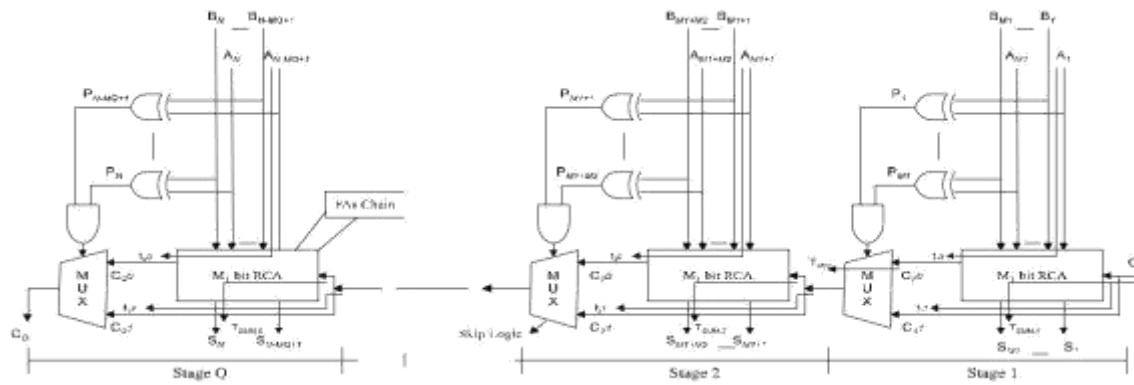


Fig 1: Conventional CSKA Structure

As Fig. 1 shows carry skip adder uses two different independent paths, one for propagating carry skip bit and second for carry-in bit. The aim of designing carry skip adder is to rise speed of the addition operation by adding propagation of carry bit around the complete adder. If we discuss about delay, then critical path delay of carry skip adder is much lesser  $O(\sqrt{n})$  than others adder like of RCA. This structure has less no of transistors hence it has short wiring length and it regular simple structure. Carry skip adder is more preferable when addition of large number of bits required.

A carry skip adder is used to speed up the wide adders. Following figure shows 4 bit carry skip adder which consist Ripple Carry Adder as a full adder, 2:1 mux and some logic gates for skip operation. There are two different outputs of RCA one is propagate signal and second is carry skip signal.

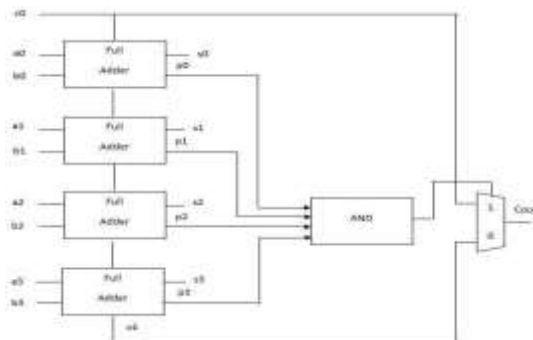


Fig.2 Four Bit Carry Skip Adder

Consider the addition of two binary digits. Ripple carry adder is depend on carry in bit which is in real carry out of previous full adder excluding the first full adder. Consider RCA for stage  $i$  then, carry in is  $C_i$  with  $C_{i-1}$  as a carry output of previous stage. Therefore, sum and carry out equations can be derived as follows:

$$\begin{aligned} P_i &= A_i \oplus B_i & .1 \\ S_i &= P_i \oplus C_i & .2 \\ C_{i+1} &= A_i B_i + P_i C_i & .3 \end{aligned}$$

Where, equation 1 shows carry propagate signal, equation 2 shows sum signal and equation 3 shows carry out signal.

#### Conventional Carry Skip Adder (CSKA)

The conventional Carry Skip Adder structure is an effectual adder in terms of delay and power reduction. Conventional Carry Skip Adder is design using chain of Full adder that is RCA block and 2:1 multiplexer. Here multiplexer is used as a connector to connect full adder block (RCA) to each other's. In Conv-CSKA structure gate and multiplexer are used to perform skip operation. Note that the carry input bit of the stage and carry output bit of its RCA block that is FA chain are used as an input of a multiplexer. Where select signal of the multiplexer is the product of propagate signal ( $P$ ). For  $N$  bit adder the  $A$  and  $B$  are the input bits that are given to the ripple carry adder along with the full adder chain. The condition of worst case delay when all full adders are in propagate mode is as given below,

$$P_i = A_i \oplus B_i = 1 \quad \text{for } i = 1, \dots, N$$

Where  $P_i$  is propagate signal associated to  $A_i$  and  $B_i$  inputs.

In this mode all Full Adders are in propagate mode and carry output of FA chain is same as carry input. When carry skip adder detect this situation then adder makes the carry output prepared for the next stage without waiting for the operation of the full adder chain to be completed.

There are two ways of implementing CSKA one is FSS(Fixed Stage Size) and second is VSS(Variable Stage Size) but higher speed can be achieve using VSS.

**Proposed Carry Skip Adder (CI-CSKA)** Proposed Carry Skip Adder is a Conventional Carry Skip Adder with some modification to get higher efficiency of Adder. The speed improvement is attained by using combine Concatenation and Incrementation Scheme (CI-CSKA) in Conventional Carry Skip Adder.

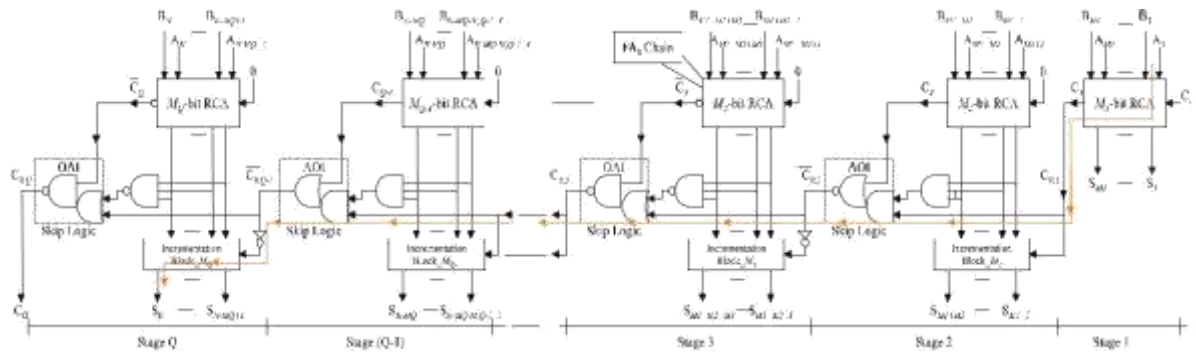


Fig. 3 Proposed CI-CSKA Structure

The proposed modified structure of the CSKA is nothing but logical replacement of 2:1 multiplexer with AND-OR-INVERT(AOI) and OR-AND-INVERT(OAI) compound gates used for the skip logic to reduce critical path delay. The reason of using compound gates is use of less number of transistors, which has small power consumption and lower path delay as compared with multiplexer which is used in Conv-CSKA. Note that, in this adder structure, when carry propagates carried out through the skip logics, they become complemented. Consequently, for even stages at the output of the skip logic, the complement of the carry is generated. The proposed adder structure has a slightly smaller area with significantly lower propagation delay as compared with the conventional adder. Internal structure of Proposed CI-CSKA contributes three parts:

- Ripple Carry Adder,
- Incrementation Block,
- Skip Logic (AOI and OAI gates)

#### a) Ripple Carry Adder

In Proposed CI-CSKA structure, the starting first stage consists only one single block that is Ripple Carry Adder. Adder consists of  $N$  bits inputs,  $A$  and  $B$ , and  $Q$  number of stages. In CI-CSKA each and every stage consists of Ripple Carry Adder with the stage size of  $Mj$  ( $j = 1, \dots, Q$ ). In Proposed structure, the carry inputs of all Ripple Carry Adder block, except the first RCA block which is  $C_i$ , is zero and because of the concatenation of full adder RCA block, all blocks execute their work simultaneously. In the working of CI-CSKA, when the ripple carry block that is the first block calculates the summation of its respective input bits that is  $SM1, \dots, S1$  and  $C1$ , then the other blocks concurrently compute the intermediate results that are  $\{ZKj+Mj, \dots, ZKj+2, ZKj+1\}$  and  $Cj$  signal.

#### b) Incrementation Block

The proposed structure consists of two blocks: RCA and Incrementation block from stage 2 to  $Q$ . The internal structure of the incrementation block is designed by using a chain of half adders (HA) as shown in the figure. While computing the final summation of the stage, the incrementation block uses the intermediate result generated by the full adder block that is the RCA block and the carry output of the preceding stage. Note that while calculating the carry output of the stage, the carry output of the incrementation block is not used to reduce the delay significantly.

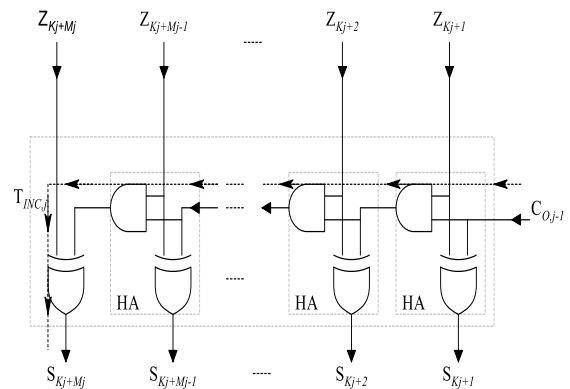


Fig. 4 Internal Structure of Incrementation Block

#### c) Skip Logic (AOI and OAI gates)

In the proposed structure, AOI (AND-OR-Invert) and OAI (OR-AND-Invert) logic compound gates are used to reduce critical path delay, which work as skip logic. The reason for using AOI and OAI gates is that they require a less number of transistors, less area consumption, have lower delay with small power consumption. The skip logic decides the carry output signal of the  $j$ th stage ( $CO, j$ ) based on the intermediate results of the  $j$ th stage and the carry output of the preceding stage ( $CO, j-1$ ). The cases may be encountered while determining  $CO, j$ . In the first case, if  $Cj$  is equal to one, then  $CO, j$  will be one. In the second case, when  $Cj$  is equal to zero, if the product of the

intermediate results is one (zero), the value of  $CO, j$  will be the similar as  $CO, j-1$  (zero). The main purpose of using both AOI and OAI compound gates is they used as a standard cell libraries as the skip logics is the inverting functions of these gates. This way in carry skip adder the need for an inverter gate, which increases the power consumption and delay, is excluded. As shown in Fig. It is noted that if, an AOI is used as

for the skip logic, then the next skip logic should use OAI gate.

AOI and OAI are constructed from combination of basic logic gates. These gates are advantageous where total number transistors (or gates) is less than if the AND, NOT, and OR functions were implemented separately. It should be noted that OAI is nothing but compliment of AOI gate.

### Simulation Results

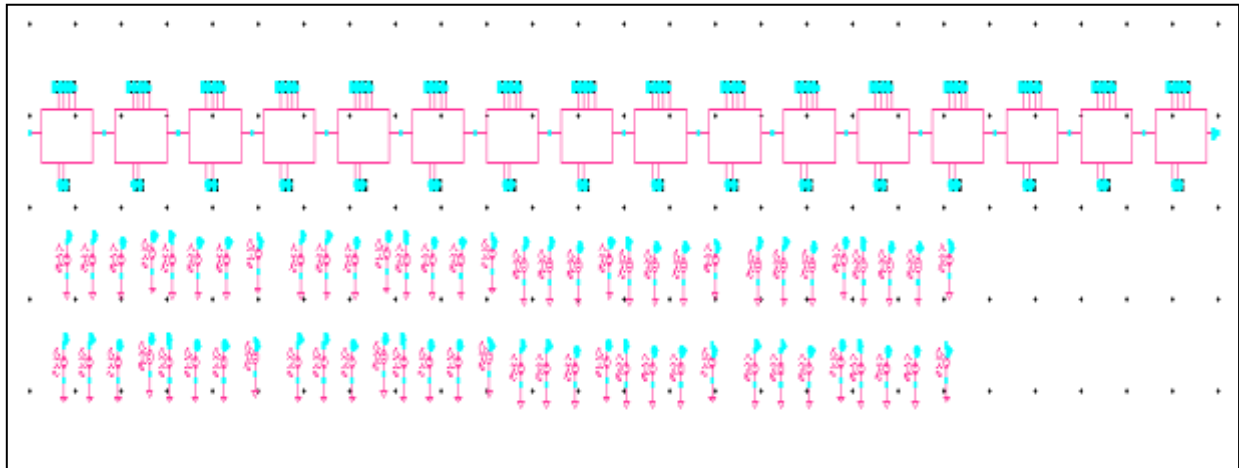


Fig 5: Schematic Structure of Conventional CSKA

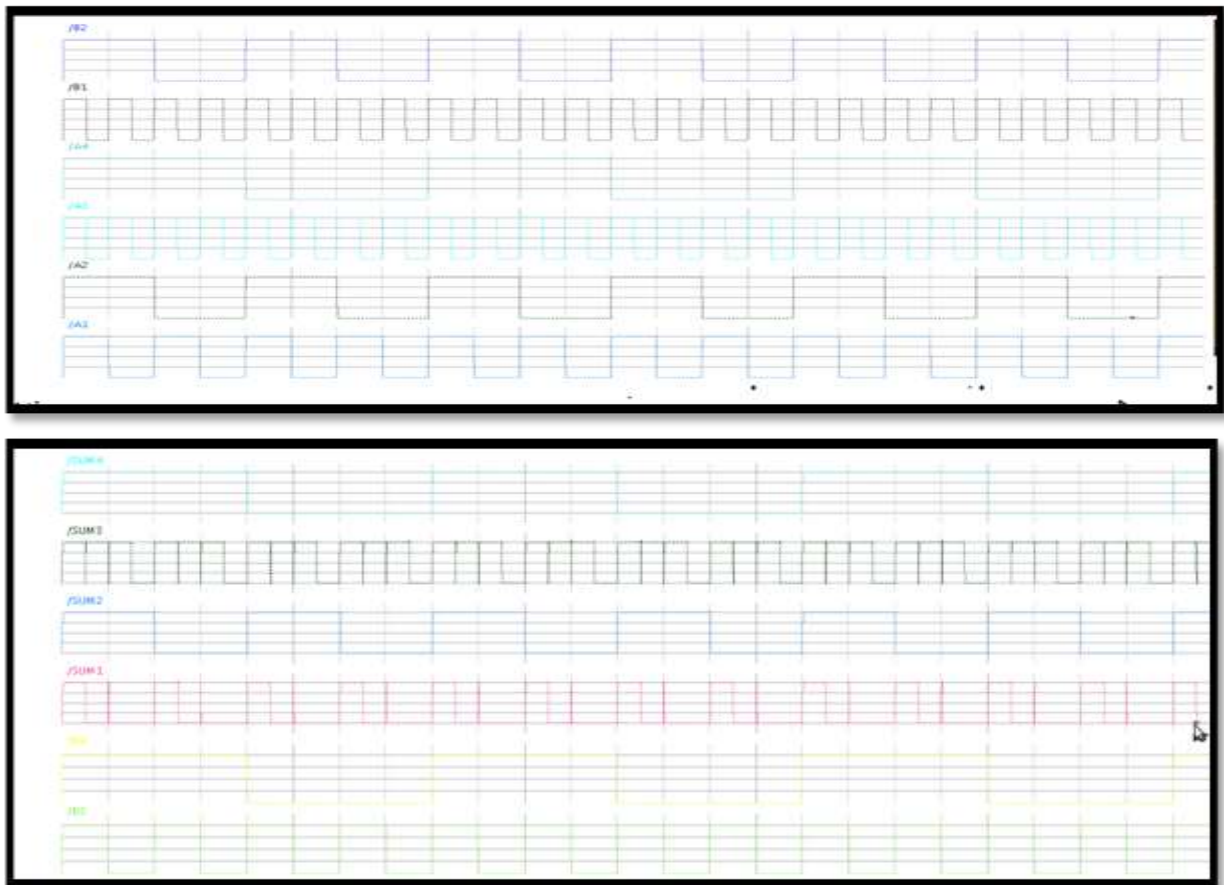
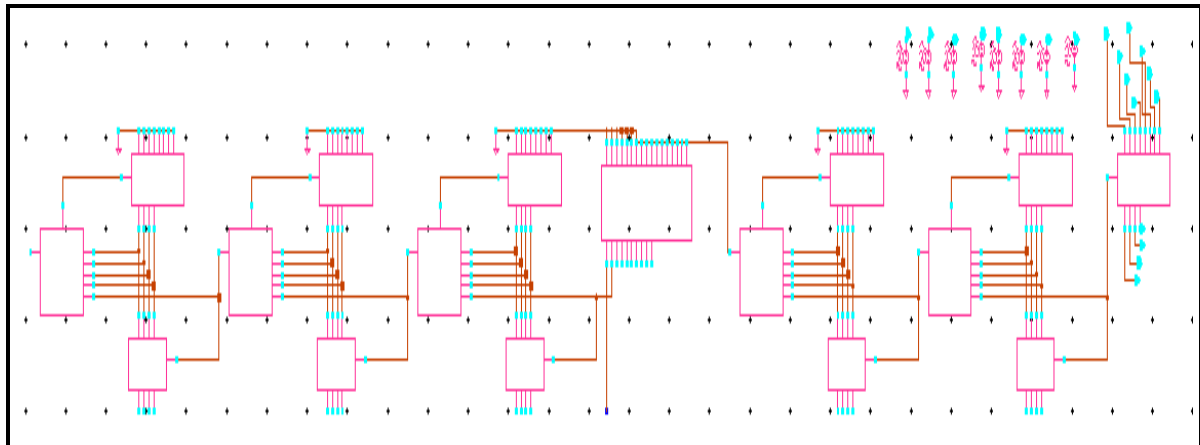
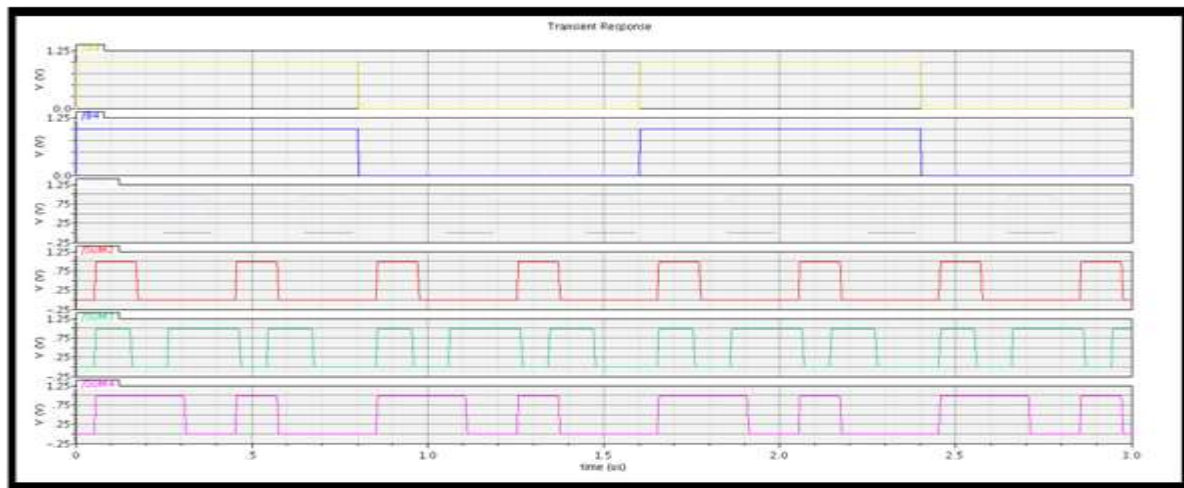
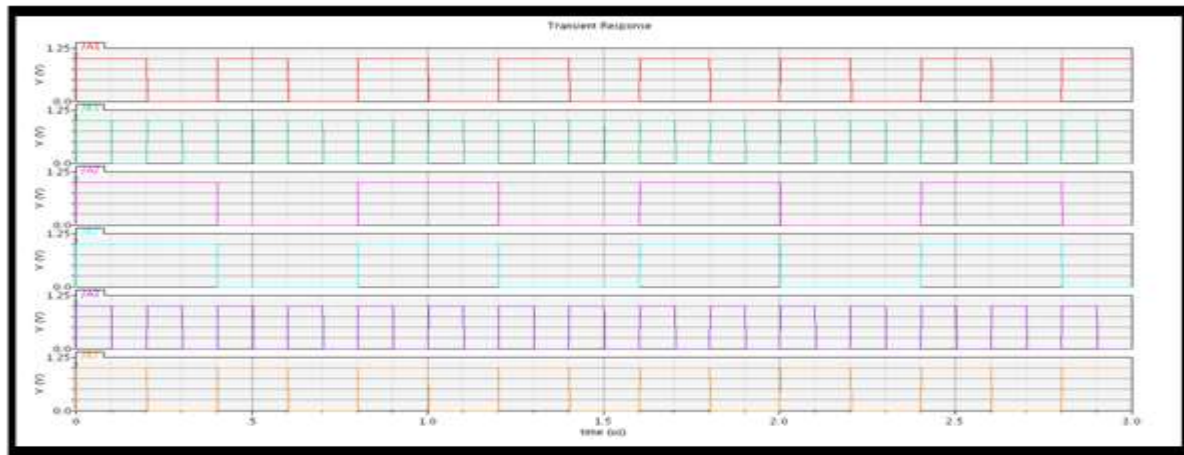


Fig 6: Simulation Result of Conventional CSKA



**Fig 7: Schematic Structure of Propose CI-CSKA**



**Fig 8: Simulation Result of Propose CI-CSKA**

| Sr. No.           | Delay(ns) | Power( uW) | Power Delay Product (PDP) |
|-------------------|-----------|------------|---------------------------|
| Conventional CSKA | 15.40ns   | 5.129uW    | 78.986                    |
| Proposed CI-CSKA  | 10.21ns   | 3.847uW    | 39.277                    |

**Table 1: Comparison Table of CSKA and CI-CSKA**

Table 1 shows comparison of Conventional Carry Skip Adder (CSKA) with Proposed Carry Skip Adder (CI CSKA) in terms of Delay and Power parameters. From the table we can conclude that delay of Proposed CI-CSKA is smaller than Conventional CSKA, hence Proposed CSKA provide higher speed as compared to Conventional CSKA. Also Power consumption of proposed structure is smaller than Conventional adder, hence proposed structure is more efficient than Conventional structure.

### Conclusion

In this project we design the Conventional Carry Skip Adder (CSKA) and Proposed Carry Skip Adder(CI-CSKA) using cadence virtuoso design tool. In CI- CSKA to enhance the speed of adder we modify Conventional CSKA by replacing 2:1 MUX by AOI/OAI compound gates and by using incrementation block. Proposed structure uses Concatenation and Incrementation Scheme for higher performance. The results shows that the CI-CSKA structure is a good adder compare to conventional CSKA for the applications where high speed and low power consumption with lower PDP are required.

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