

Design of Lookup Table using Quaternary Logic in Voltage Mode Standard CMOS Circuit

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Abstract

Designers face challenges in interconnection due to the large number of components. Interconnection and power consumption perform significant part in this paper. The shortcomings of the previous work done is high interconnections, which leads to high power usage along with more area required. The Binary logic circuits are constrained by using the number of interconnections, which increases the delay and power consumption with the boom in logic. So we design new techniques that are going to reduce the interconnection of the circuit as well as the power consumptions. Multiple-valued logic can decrease the number of required interconnections. In this paper we use quaternary to binary decoder to reduce the multiplexer control lines. The vital parts of the processing component and therefore it has a focal point of research. Therefore, the design of adders through multiplexer using multi-valued logic can show to be very beneficial. So we introduce and full adder based totally at the designed quaternary lookup table.

Keywords: Quaternary Look-Up Table, Multi-Valued Logic, Standard CMOS Technology

Introduction

In Traditional binary CMOS advanced circuits, static power utilization has its linkage to outflow current, and dynamic power consumption is given by equation 1 given underneath (1), where C is the capacitance of the node being determined and V_{DD} is the power supply voltage

$$P_D \propto CV_{DD}^2 \quad \text{-- (1)}$$

The CMOS process moved a long way by shrinking the transistors (thus dropping C) and using lower supply voltages (Reduced V_{DD}), leading to low power and high integration scenario. This capacitance C includes the directing capacitance of interfacing wires as well. It has been stated that routing overstep transistors impact for latency and power dissipation of design in current CMOS forms [1]. This becomes quite critical in FPGA'S where the power where the power used in

directing may reach up to 70% of general utilization [2]. FPGAs have turned out to be a very integral part of modern day digital system design as they give a good cost to performance ratio when equated to application-specific integrated circuits (ASICs) One approach to limit the influence of interconnections is to use multi-valued logic (MVL) [3], henceforth, more data can be conveyed in every single wire, decreasing the routing system. Therefore, only one wire conveying a signal with N logic levels can displace $\lceil \log_2 N \rceil$ wires conveying binary signal. With interconnection being reduced it ultimately leads to reduction in line capacitance and the overall area used. This also leads to reduced power consumption on account of logic levels coming close to each other. The new power consumption can be dictated by (2)

$$PD \propto CV_{DD}V_{avg} \quad \text{-- (2)}$$

Where V_{avg} is the average voltage distance between levels of logic. However MVL has a comparatively low noise margin than binary. While there is still a scope for power and space optimization it is expected that MOSFET shrinking will soak as transistors approach the atomic dimensions, forcing a basic hindrance. These downsides have kept MVL non-competitive as compared to binary logic. [1] In this work we plan to outline a Quaternary look-into table structure, to substitute or supplement binary lookup table in field programmable gate array. The circuit is flawless with standard CMOS shapes, with only voltage supply and using simply essential voltage mode structure. A clock boosting system is utilized to enhance the switches resistances and power utilization. A quaternary variable can expect four diverse logic levels. The quaternary variable (Q) can convey double as much data as a binary variable (B), we have the succeeding relation:

$$|Q|=2x|B| \quad \text{-- (3)}$$

Two binary variables might be gathered into one quaternary variable minus data loss, combining two

nodes into one. It ought to be noticed that there is no immediate transformation of binary to quaternary logic in regular CMOS, as the binary circuits utilize the accessible power rails to represent to the binary symbols. [1]

Quaternary Look up Table

The proposed QLUT is as given in fig 1.

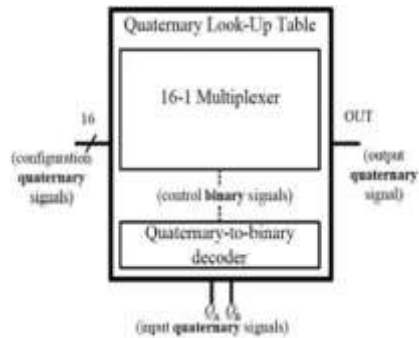


Fig1-Quaternary look-up table[1]

The proposed work can be explained as below

For the complexity of QLUT indicated it is fundamental to have 16 quaternary arrangement at a rate of one configuration for every conceivable combinations of two quaternary input. The arrangement here means the reconfigurable quaternary capacity. By and large the information signals are utilized to choose which one of the arrangement inputs is associated with the yields. The propose QLUT is made out of two block: 16-1 multiplier utilizing a variety of switches that sets up a low-resistance way between one setup input and the output as per the input esteems.

Quaternary-to-binary decoder comprising of a 2 bit analog to digital (ADC) fronted took after by combinational logic is used to accomplish the control signal aiding the multiplexer.

QLUT Implementations

The design was incorporated utilizing a standard CMOS innovation, wherein a solo supply of voltage and clock boosting circuit is utilized to combine a 16 to 1 multiplexer and a quaternary to binary decoder. The circuit has two quaternary input, Q_A and Q_B which are then registered by the quaternary to binary decoder into the QLUT's binary control signals, CS1-CS16. The multiplexer 16-to-1 consists of sixteen NMOS switches improved with a clock boosting circuit. When single control signals is high, the comparing Quaternary lookup table line-switch-is initiated associating the relating QLUT's quaternary contribution to the output. The four voltage level is given underneath.

Voltage Level	Corresponding Voltage value in volts (V)
0	0 Volts

1	0.4 Volts
2	0.7 Volts
3	1 Volts

Table I: Table Showing Four Voltage Level

A Lookup table is an array indexing operator where the output is plotted by the input, built on the configuration memory [1].The configuration values are at first put away in the LUT design memory, and as indicated by the input, the logic value in the tended to position is appointed to the output.

a) 16:1 MUX

The mux used here's a 16x1, so it has 16 input pins and 1 output pin. This mux has usually four control lines in binary logic. Through the usage of the quaternary logic, the control lines are reduced to two. This is done with the brand new quaternary to binary decoder part introduced in the lookup table. The decoder reduces the fetch line of the mux from four to two. We choose mux for this purpose so that we can design a mux into an adder, subtracter, and divider or can use it for any other arithmetic or logical functions. The look up table will guide the mux to do various operations. The mux used has 16 pins, so we have switches that need to be operated very speedy to get the correct output. In the proposed method, here we use the direct technique to do the work in a single clock cycle.

b) Clock Boosting Technique

Clock boosting is the important technique for reducing the interconnection problem and increase speed with reduced delay. Expecting that the capacitor C is released and clk_1 is set to logic 1 (V_{DD}), N1 turns on and interfaces node B to ground, while P1 off and guarantees a high impedance way between the node A and B. All the while, P2 is on and step by step charges the capacitor (and node A) to V_{DD} . At the point when clk_1 drives to a logic 0 (ground), N1 off; the inverter ties the capacitor base plate to V_{DD} and P2 off; node Emerges to $2V_{DD}$ and P1 is turned on interfacing node B to $2V_{DD}$ as needed appeared in fig2:[1]

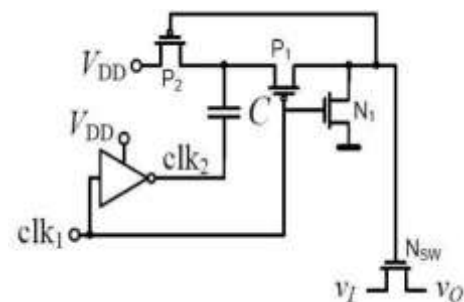


Fig 2: Proposed Transistor Level Schematic [1]

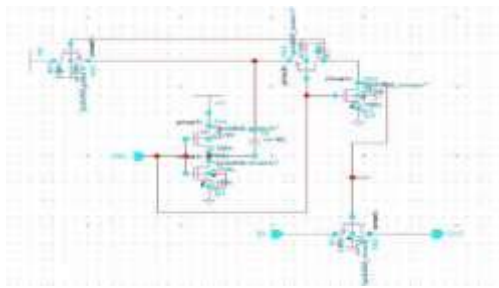


Fig 3: Transmission Gate Diagram

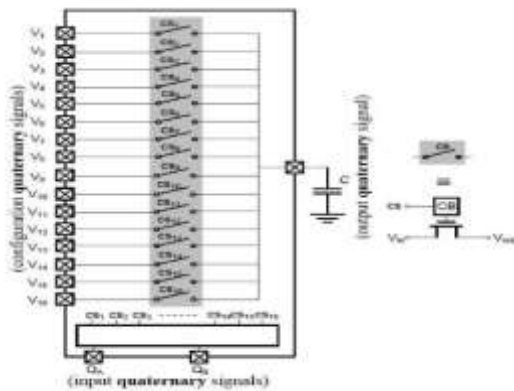


Fig 4 Quaternary Lookup Table [1]

c) Quaternary to Binary Decoder

The 2-bit quaternary-to-binary decoder permits the utilization of a single line of switches to initiate the input arrangement signal to the output of the quaternary lookup table. And to do as such we create 16 control signals, which is connected in the clock1 contribution of every single switch, showed up in fig2 these switches are endeavoring to associate one quaternary arrangement contribution to the output. [1] To convey the essential control flag, the quaternary elements are decoded into binary, allowing the use of binary logic gates We have utilized Flip-flopping self-referenced comparators, where QA and QB is a quaternary input of the QLUT. Where the binary signal and their complement are connected to a combinational logic block incorporated only by NAND gates. The combinational block is utilized to create the one hot coded yield cs , which is at utilized to pick and turn on just a single switch amid the 16 accessible in the quaternary lookup table.[1]

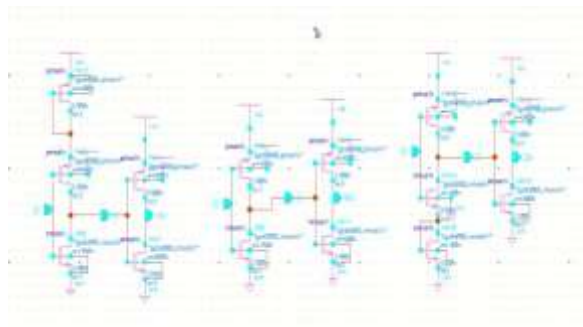


Fig 5- Self Inverting Referenced Comparator

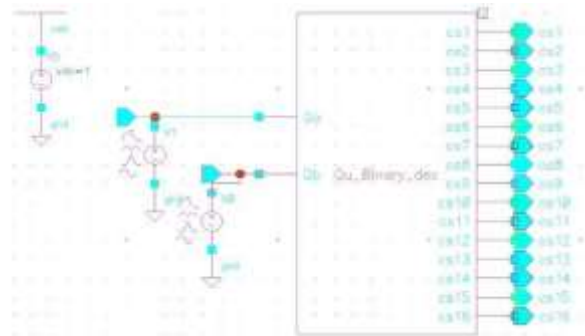


Fig 6: Quaternary to Binary Decoder

Simulation and Results

A) QLUT Half Adder and Full Adder

Adder is just a model it explain the logical function of quaternary logic. The adder designed using mux is used. The half and full adder circuit are presented here. The truth table and the results obtained are discussed further. In logic, quaternary expansion can be performed from various perspectives. Numbers in quaternary logic can be specifically included or numbers in quaternary logic can be changed over this binary logic and expansion can be performed in binary logic. Binary aftereffects of expansion can be shown in quaternary logic after conversion.

Table III exhibits the full adder truth table. It may be accumulated that the outcomes for the Sum and COUT signals may be viably overcome logic move on input. The shift block is executed for one of the input and plays out a signal up-move on a quaternary input values. Using the two quaternary lookup table outlined with the results when C_{IN} is 0, as showed up in table III, it is watched that the result with C_{IN} can be gotten, for the Sum, by climbing one level on QB . For COUT same logic can be performed prompting an up move of one level on the variable QA which thinks about to a move of four levels on the COUT output, with uncommon situation when QA has level 3, which is dealt with by joining the Y_c and Z_{in} (which are 0 when C_{IN} has the level 1 and QA has the level 3) on a NOR to device the 2-1 multiplexer.

This block is executed with two 2-input NAND gates, 4 inverters and two 2-input NOR gates. The expected logic to play out the shift and to decode the C_{IN} is added to the quaternary lookup table. These block are completed stabilizing power and area as low as could be permitted while satisfying the delay limitation. Also, to change over the quaternary variable C_{IN} into binary, we incorporated a comparator CP and an inverter to the comparators frontend. [1]

Here the fig7. And fig9. Are the quaternary half and full adder.

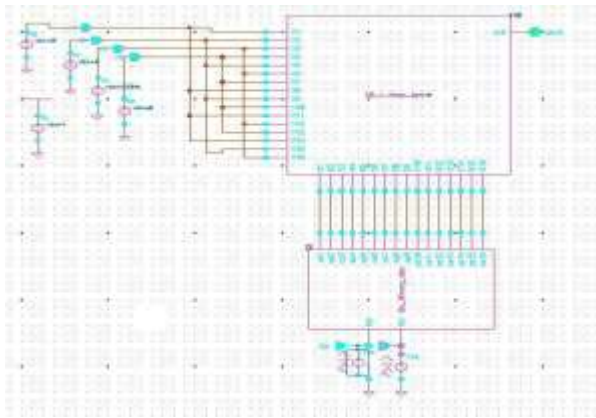


Fig 7: Implementation of QLUT Half Adder

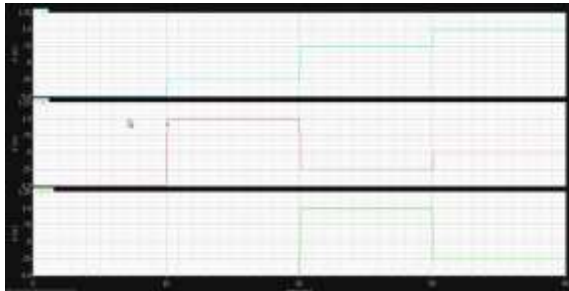


Fig 8: Waveform of QLUT Half Adder

QA	0 ₄	0 ₄	0 ₄	0 ₄	1 ₄	1 ₄	1 ₄	1 ₄	2 ₄	2 ₄	2 ₄	2 ₄	3 ₄	3 ₄	3 ₄	3 ₄
QB	0 ₄	1 ₄	2 ₄	3 ₄	0 ₄	1 ₄	2 ₄	3 ₄	0 ₄	1 ₄	2 ₄	3 ₄	0 ₄	1 ₄	2 ₄	3 ₄
Sum	0 ₄	1 ₄	2 ₄	3 ₄	1 ₄	2 ₄	3 ₄	0 ₄	2 ₄	3 ₄	0 ₄	1 ₄	3 ₄	0 ₄	1 ₄	2 ₄

Table II – Truth table of half adder [1]

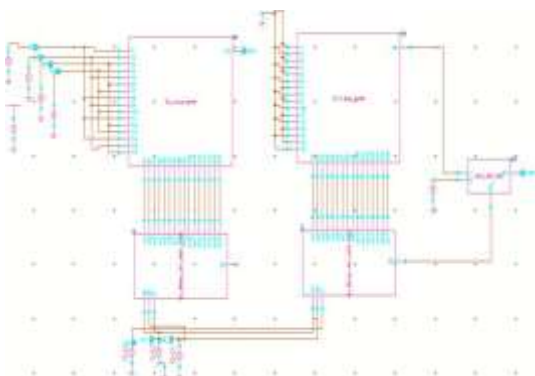


Fig 9- Implementation of QLUT Full Adder



Fig 10- Waveform of QLUT Full Adder

QA	QB	CIN	Sum	COUT	QA	QB	CIN	Sum	COUT
0 ₄	0 ₄	0 ₄	0 ₄	0 ₄	0 ₄	0 ₄	1 ₄	1 ₄	0 ₄
0 ₄	1 ₄	0 ₄	1 ₄	0 ₄	0 ₄	1 ₄	1 ₄	2 ₄	0 ₄
0 ₄	2 ₄	0 ₄	2 ₄	0 ₄	0 ₄	2 ₄	1 ₄	3 ₄	0 ₄
0 ₄	3 ₄	0 ₄	3 ₄	0 ₄	0 ₄	3 ₄	1 ₄	0 ₄	1 ₄
1 ₄	0 ₄	0 ₄	1 ₄	0 ₄	1 ₄	0 ₄	1 ₄	2 ₄	0 ₄
1 ₄	1 ₄	0 ₄	2 ₄	0 ₄	1 ₄	1 ₄	1 ₄	3 ₄	0 ₄
1 ₄	2 ₄	0 ₄	3 ₄	0 ₄	1 ₄	2 ₄	1 ₄	0 ₄	1 ₄
1 ₄	3 ₄	0 ₄	0 ₄	1 ₄	1 ₄	3 ₄	1 ₄	1 ₄	1 ₄
2 ₄	0 ₄	0 ₄	2 ₄	0 ₄	2 ₄	0 ₄	1 ₄	3 ₄	0 ₄
2 ₄	1 ₄	0 ₄	3 ₄	0 ₄	2 ₄	1 ₄	1 ₄	0 ₄	1 ₄
2 ₄	2 ₄	0 ₄	0 ₄	1 ₄	2 ₄	2 ₄	1 ₄	1 ₄	1 ₄
2 ₄	3 ₄	0 ₄	1 ₄	1 ₄	2 ₄	3 ₄	1 ₄	2 ₄	1 ₄
3 ₄	0 ₄	0 ₄	3 ₄	0 ₄	3 ₄	0 ₄	1 ₄	0 ₄	1 ₄
3 ₄	1 ₄	0 ₄	0 ₄	1 ₄	3 ₄	1 ₄	1 ₄	1 ₄	1 ₄
3 ₄	2 ₄	0 ₄	1 ₄	1 ₄	3 ₄	2 ₄	1 ₄	2 ₄	1 ₄
3 ₄	3 ₄	0 ₄	2 ₄	1 ₄	3 ₄	3 ₄	1 ₄	3 ₄	1 ₄

Table III- Full Adder Truth Table [1]

We have calculated the power and area of proposed implementation of half adder and full adder.

Parameters	Half adder	Full adder
Power	1.12 mW	3.08 mW
Area (trans. Count)	172	356

Table IV- Parametric Analysis of Half Adder and Full Adder

Conclusion:

Voltage Mode CMOS multivalued design understanding using quaternary lookup table (QLUT) gain attention due to its striking characterization and performance factor. The proposed design of half adder & full adder using quaternary logic has better function as compared to binary logic. The transistor count is less and the power dissipation is 1.12 mW for half adder and 3.08mW for full adder.

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