

For the required voltage swing at very low tail bias currents, very high load resistor which occupies less area is required [5]. This resistance can be adjusted by the bias voltage V_{bp} to get the required tail bias current. For this purpose small sized PMOS transistors with their bulk and drain connected are used as load resistors. From the below equation 1 it is understood that the output voltage swing depends on load resistor R_L

$$V_{SW} = V_{OH} - V_{OL} = 2 R_L \cdot I_{SS} \quad (1)$$

For a fixed tail bias current, R_L can be controlled by the aspect ratio of PMOS Transistor.

$$\text{Power dissipation} = V_{DD} \cdot I_{SS} \quad (2)$$

The Output Time Constant is given by

$$\tau_{CML} = R_L \cdot C_L = V_{SW} / I_{SS} \cdot C_L \quad (3)$$

where C_L is Total Output Capacitance.

The Power Delay Product is given by

$$PDP_{CML} = \ln(2) \times V_{DD} \times V_{SW} \times I_{SS} \times C_L \quad (4)$$

Basic CML logic gates like NAND/AND, NOR/OR, XOR/NOR can be designed with the help of Binary Decision diagrams. The logic operation of the gates is implemented in the NMOS differential pairs. With reference to Binary decision diagrams, each node acts as a differential pair and every branch represents the connection between the drain and the source of the output [4].

VCO Based ADC Design

The fundamental building blocks of numerous Electronic Systems are Analog to Digital Converters (ADC). Recent Mixed Signal Integrated Circuits (ICs) (which is a combination of analog and digital) circuits are composed of a Digital Signal Processor (DSP) core which constitutes input interfaces to the external analog signals by using ADCs. The boost in the hand-held and battery operated Electronic Systems is aspiring designers to sort for ADC architectures which endeavor lower power consumption and are farther cost-efficient.

Lately in the Mixed Signal Community, Voltage Controlled Oscillator (VCO) Based Analog to Digital Converters (ADCs) have become an elaborate content of interest. It is also called as VCO-based Quantizer or Frequency Delta-Sigma Modulator (FDSM) as it is a time-based architecture which transform an analog input signal into time information and then the time information to Digital Output signal. It can be accomplished by using VCO and Digital circuits [8].

VCO based ADC was initially used in Delta Sigma Modulators. It is used in numerous applications like Positron Emission Tomography, Signal Acquisition and Processing Applications. VCO based ADC chiefly consist of Voltage Controlled Oscillator, Reset Counter and Adder. VCO creates an output signal whose frequency is proportional to the input analog signal. The Reset Counter counts the output clock pulses from VCO for individual rising edge of the clock. The adder adds the output clock pulses of the reset counter and ultimately gives the digital output

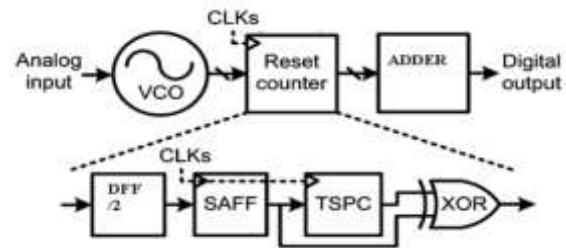


Fig 2: Block diagram of VCO based ADC

A. Voltage Control Oscillator

It is an oscillator which converts the input signal into the corresponding output signal. As the input signal controls the output frequency, the input signal is denoted by V_{ctrl} . VCO behaves as a CT Integrator with infinite DC gain as it produces output phase endlessly even for a DC gain. In this design, VCO is designed using CMOS ring oscillators. Operation of ring oscillator is based on the delay existing between input and output of the inverter.

Ring oscillator frequency depends on the number of delay stages and the delay caused by them. Ring oscillator has number of amplifiers in a feedback loop. As each amplifier stage acts as an inverter, it will delay the signal with time t_d and hence referred as delay cell. Natural frequency of oscillation can be obtained if odd number of inverters are connected in cascade.

Ring oscillator delay cells are designed using either single ended or differential topology. Differential ring oscillators are preferred as they are independent of PVT Variations, have low power and minimizes the noise. The load element in the differential VCO is cross coupled PMOS transistors which guarantee the differential operation of the delay cell. Auxiliary PMOS transistors are also used for controlling the oscillation frequency. The circuit is designed using eight differential delay cells to get the required output frequency. It can also be called as 8 stage /16 phase ring oscillator [9]

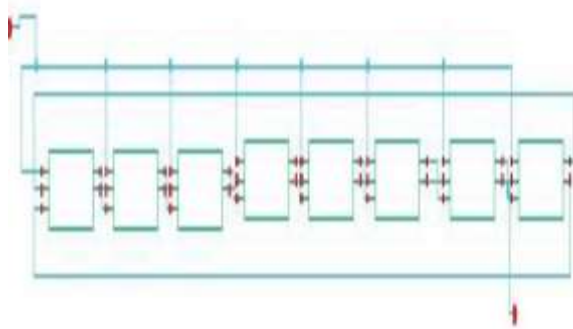


Fig 3: Schematic of 8 Stage Ring Oscillator

B Reset Counter

This counter is implemented using different flip flops. The Reset Counter consists of one divided by 2 flip flop, two DFFs and an XOR gate. The Divider uses a general DFF, the first DFF uses a Sense Amplifier Based Flip flop (SAFF) to reduce the noise while the second DFF uses a True Single Phase Clock flip flop (TSPC) to reduce power consumption and an XOR Gate is used to reset the counter. Each rising edge of the clock is counted by the counter.

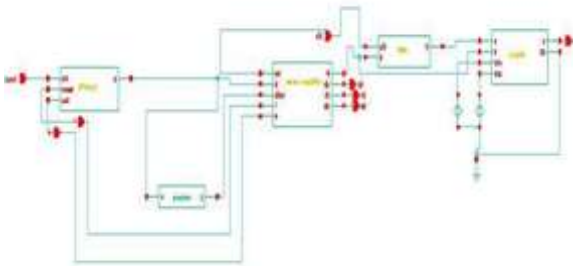


Fig 4: Schematic of Reset Counter

C Divided by 2 flip flop

The circuit operates by feeding back from Q to the input terminal D as shown in the fig 5 below. The output pulses at Q have a frequency exactly one half of that of the input frequency. D Flip flop can be used as binary divider for frequency division or as divide by 2 counter. This flip flop is designed using source coupled logic in sub threshold region [7]

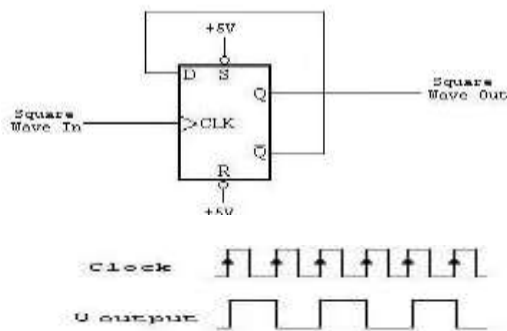


Fig 5: Divided by 2 D flip flop

D Sense Amplifier based Flip Flop

This Flip flop can be used for high performance and low power digital. It has very small delay and works with low swing differential inputs. These flip flops have differential outputs and differential inputs. In the designed SAFF Circuit the first stage is differential input differential output sense amplifier which works as a pulse generator while the second stage is NAND based Cross coupled SR latch which acts as a slave.

Sense amplifier senses the true and complementary differential inputs and produces transitions from high to low logic level on one of the outputs. SR Latch captures each transitions and holds the state until the next leading clock edge arrives. Thus it acts as a flip flop.

E TSPC Flip Flop

The True Single Phase Clock (TSPC) is a familiar Dynamic Flip Flop which fulfills the flip-flop operation at high speeds and with less power. In the design of TSPC flip-flop, Edge Triggered (positive or negative) D flip-flop is used. The circuit constitutes of alternating stages called n-blocks and p-blocks and individual block are being driven by the same clock. In this design, a single global clock signal needs to be yielded henceforth, it is competent for both static and dynamic CMOS circuits. Here a Positive Edge Triggered TSPC D-flip-flop is used which conducts when the clock signal clock is LOW and the input is isolated from the output. When clock makes a LOW to HIGH transition, the output will latch the complement of the input.

The true single phase clock dynamic CMOS circuit employs only one clock signal for synchronization and it also restricts the complexity. The clocking system in the design may have single phase clock or multiple phase clocks. The clock phase controls the transfer of data between clock storage devices used in the synchronous VLSI digital systems. The output is same as input at both the rising and falling edge of the clock signal

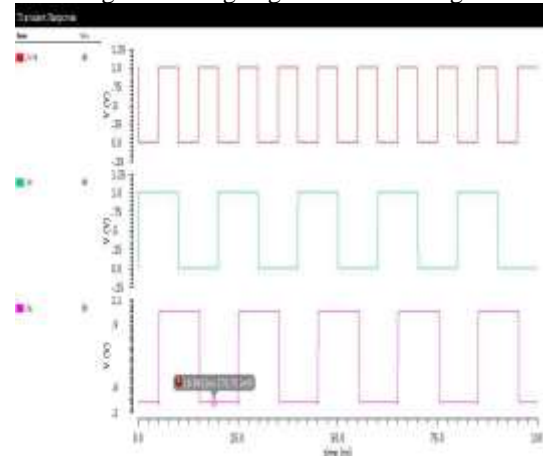


Fig 6: Output of TSPC Flip flop

F Carry Save Adder

The Implementation of a High Speed Multi Operand Adder is Carry Save Adder (CSA). A Carry Save Adder constitutes of a ladder of stand-alone Full Adders. The n-bit CSA consists of n disjoint full adders (FAs) where each adder calculates a single sum and carry bit based on the resemblant bits of the three input numbers. It devours three n-bit input integers and yields two outputs, n-bit partial sum and n-bit carry. Unlike the ripple carry adder, CSA consists of multiple one-bit full adders without any carry chaining [6]

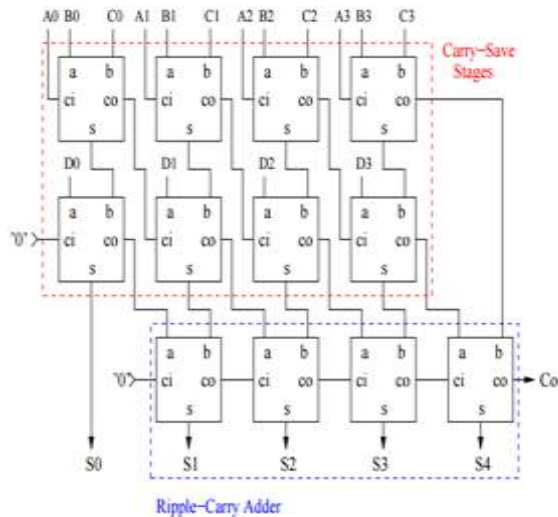


Fig 7: Carry Save Adder

Results and Discussion

A. Circuit Implementation

The output of VCO is a pulse whose input control voltage is proportional to the output frequency. The counter is used to count the number of rising edges (and thus the frequency) that is generated by the VCO for a particular input signal during the sampling clock period. At the end of every period, the counter value is read out by a sampling register and the counter is reset to zero. By comparing samples of the current and previous states with XOR gate and 2 flip flops, the number of elements in the ring oscillator that undergoes a transition with a given sampling clock period can be noted [10]

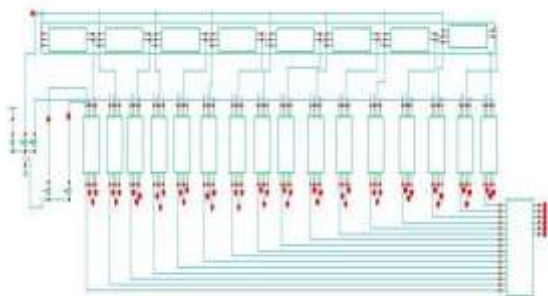


Fig 8: VCO based ADC Design

The output of the XOR gate is given to the clock of the first flip flop. A reset signal is used to reset the counter after every 100 n sec. The final count after every 100 nsec is stored in the chain of D flip flops. The adder adds the outputs from the reset counter and finally gives the digital output.

In the design the blocks like XOR gate, D flip flop, Carry Save Adder are designed using CML technique. VCO Based ADC is Designed at a supply voltage of 1V in 45nm technology using cadence virtuoso tools.

B. Results

The simulation results of VCO based ADC with CML Technique in 45nm technology using Cadence virtuoso tools for a power supply of 1V are presented. The outputs of VCO, Reset Counter and VCO based ADC are shown from fig 9 to fig 11.

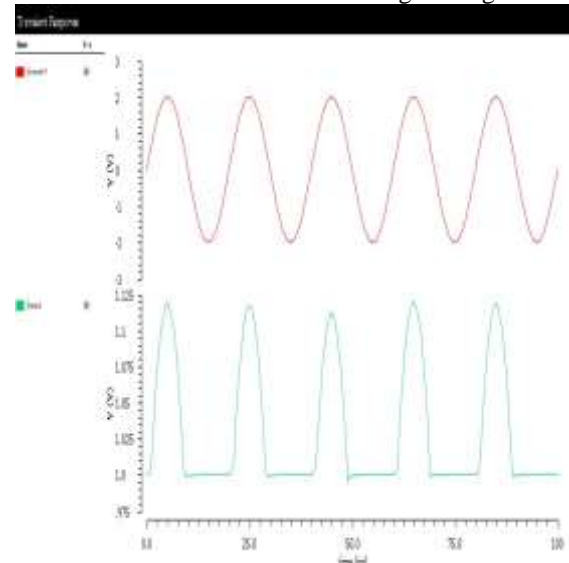


Figure 9 Output of VCO

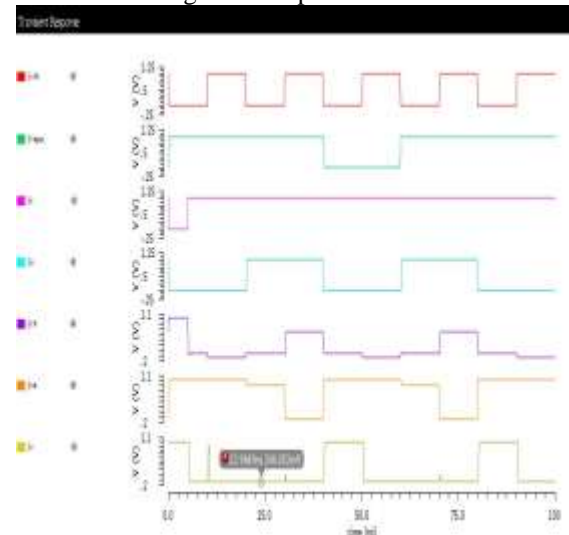


Figure 10 Output of Reset counter

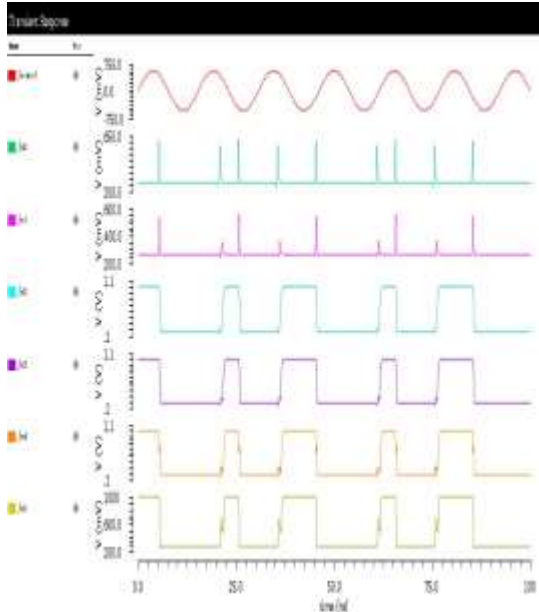


Figure 11 Output of VCO based ADC

TABLE 1: Power and Delay of Basic Gates in 45nm Technology at VDD =1V

Basic Gates	CMOS		CML	
	Power (W)	Delay (sec)	Power (W)	Delay (sec)
Inverter	5E-3	30.4E-6	7.28E-6	25.32E-12
OR	16.69E-9	20.24E-9	18.76E-6	19.88E-12
AND	10.92E-9	20.16E-9	22.96E-6	10.04E-12
NOR	7.26E-9	84.12E-12	18.76E-6	10.1E-9
NAND	7.51E-9	39.54E-12	22.9E-6	28.33E-12

The power and delay of CML gates is calculated and compared with CMOS basic gates which is given below in the table 1 at power supply of 1V and table 2 for a power supply of 0.5V for both techniques. It is found that using CML technique the power is reduced when compared with CMOS at different supply voltages.

TABLE 2: Power and Delay of Basic Gates in 45nm Technology at VDD =0.5 V

Basic Gates	CMOS		CML	
	Power (W)	Delay (sec)	Power (W)	Delay (sec)
Inverter	201E-12	11.41E-9	100.1E-12	2.73E-9
OR	351.5E-12	20.24E-6	7.54E-9	28.64E-6
AND	38.26E-12	20.21E-6	1.26E-9	39.23E-6
NOR	339.9E-12	6.43E-9	7.54E-9	17.48E-6
NAND	37.3E-12	32.28E-9	1.26E-9	10.09E-9

The power and delay calculations of different blocks of VCO based ADC using CML Technique is given in table 3 below. It is understood from the table that power is reduced with CML technique and the performance is good when compared to conventional CMOS logic.

TABLE 3: Power and Delay of Different VCO based ADC Blocks

	Power (W)	Delay(sec)
VCO	128.9E-12	7.78E-9
RESET COUNTER	32.06E-3	5.28E-9
DIVIDED BY 2 CIRCUIT	18.33E-3	228.8E-12
TSPC	6.03E-6	5.06E-9
SAFF	9.16E-3	10.25E-9
XOR Gate	121.3E-3	45.245E-9
Carry save adder	109.6E-3	28.089E-9
VCO Based ADC	622E-3	484.5E-12

Conclusion

By designing the VCO Based ADC using current mode logic (CML) digital logic gates in transistor level schematic are designed and operated at a bias voltages of V_{BN} of 0.5V and V_{BP} of 0.8V with VDD of 1V power supply. In CMOS technology, the logic levels for logic 0 is 0V and logic 1 is 1V but in the case of CML logic by using these above bias

voltages the output of the logic levels for logic 0 is 0.248V (voltage swing) and logic 1 is 0.96V which is an advantage. Another advantage of CML compared to CMOS is the number of transistors will be less, it has less delay so more speed of operation and also consuming very low energy per computation. Thus the CML-based digital systems are highly suitable for designing the digital parts of the VCO Based ADC. The schematics are drawn using cadence virtuoso, schematic editor, symbol editor and while the simulations are done using Analog design environment (ADE L) Tools. The overall power and delay of VCO based ADC is 622.7mW and 484.5ps.

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