

Design of 32 Bit Data path Unit of ARM7 Microprocessor using Sub threshold Current Mode Logic

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Abstract

In the present days, Very Large Scale Integration (VLSI) is focused upon designing energy efficient electronic devices. These are nothing but the embedded gadgets whose core is a processor. Advanced RISC Machine (ARM) is one of the families of computer processors which have an reduced instruction set architecture. Current Mode Logic (CML) is one of the low power logics which is used to design circuits with an extended battery life. The circuits built using this technique are capable of giving a dependable and sturdy system. In this paper, the proposed ARM7 microprocessor has been designed using the Sub threshold Current Mode Logic (STCML). All the design blocks operate in the sub threshold region at 0.24V power supply. The Data path of ARM7 has been implemented using Cadence Virtuoso Tool in 45nm technology. The results of the blocks have been viewed on Spectra Simulator and the power and delay calculations have been computed. The propound microprocessor is capable of finding place in DSP and other Embedded applications.

Keywords: ARM7 microprocessor, CMOS, Current Mode Logic, Data path, RISC processor, STCML, VLSI

Introduction

power Dissipation is a major issue in most of the VLSI circuits whose cause is increased leakage currents and with the increasing number of transistors per unit area, this becomes more prominent. This might lead to large amount of heat-dissipation from the device which may cause its failure. When the low power application of devices is kept in view, RTL level optimization is required.[1] This is essential to obtain portable devices and those which have longevity in terms of battery life.

The CMOS technology contributes to large number of leakage currents in the transistor out of which Sub threshold leakage current is predominant. This leakage current contributes to the major part of the power dissipated by the transistors. Current Mode Logic (CML) also known as Sub threshold Source Coupled Logic (STSCCL) helps the digital circuits to be operated in sub threshold region with reduced

leakage currents and meager power consumption.[2],[3]

Microprocessors also known as single chip computers are the elementary units of information systems. Their performance has been driven by the transistor speed, energy scaling and also by the micro architecture gains advances. These advanced micro architectures have stationed transistor integration capacity, pipelining etc. to furnish increasing performance.

ARM microprocessors are the most ubiquitously used Instruction Set architectures in terms of quantity produced. ARM architects the insidious intelligence that is transfiguring our daily experience. In the world, more than 95% wearable's work on ARM delivering advanced signal processing capabilities. With the integration of ARM and low power logic, energy efficient devices which meet innovative market demands can be developed.

This paper is formed as follows Section II presents the literature review on Current Mode Logic, STCML and ARM7 Section III presents the Implementation of Datapath components of ARM7, Section IV furnishes the Simulation Results of all the Data path blocks of ARM7 in Cadence Virtuoso Tool and also the Comparison of Power and Delay with voltage scaling is presented. Finally, Section V draws the Conclusions for the proposed methods.

A. Traditional CML Topology

The logic working in an CML gate takes place in the current domain and hence the operating speed is innately high. The Fig. 1, shows a logic network where an source coupled differential pair of NMOS switches, directs the tail current (I_{SS}) to one of the output sections hinging on the logic levels of input. The output load resistance (R_L) converts this current to voltage in order to impel the following CML gates. The output voltage swing ($V_{sw} = R_L \times I_{SS}$) should be excessive enough to transform completely the input differential pair of the subsequent stage. This output voltage swing is directly proportional to the value of R_L . Hence, only when the tail current I_{SS} and output impedance is higher than the leakage currents at the junction and load resistance respectively, this circuit can perform appositely

even in assertively scaled deep submicron technologies. [3]

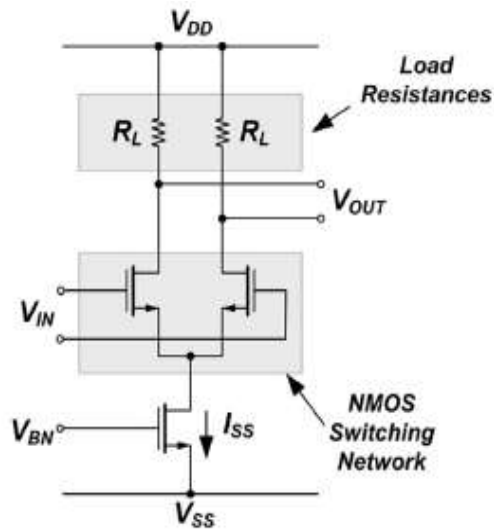


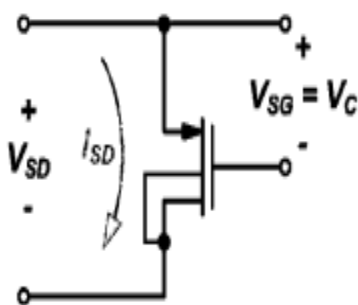
Fig.1 Standard CML Topology based inverter/buffer

The load resistances in the Fig.1 can be replaced by PMOS transistors operating in triode region. The operating speed in an SCL gate is given by,

$$T_{SCL} = R_L \times C_L = V_{sw} \cdot C_L / I_{SS} \quad (1)$$

B. STCML Gates

In the Sub threshold operation, the tail bias current would be in the range of few nA or less. So, to obtain a reasonable voltage swing at the output, R_L should be in the range of $M\Omega$. This resistance can be



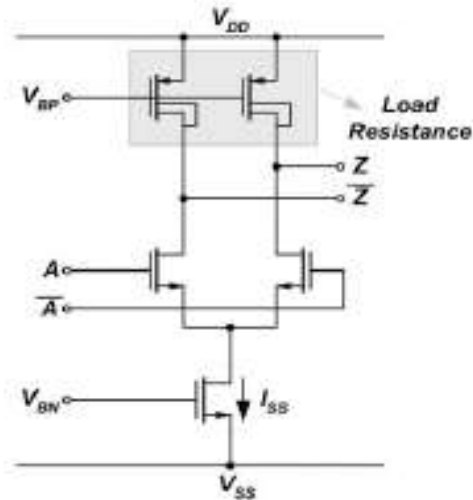
controlled by I_{SS} . Hence, a well-regulated high resistivity device having very small area is required.

Fig.2 PMOS as load device.

Hence, a very high resistivity load device can be implemented using a single PMOS transistor. Since, the devices are of minimum size, the parasitic elements associated. Fig. 2 shows limited and governable differential resistance, which can provide a limited amplitude and gain.[3],[4]. Since, the devices area of minimum size, the parasitic elements associated with the circuit can be ignored. The proposed STCML gate can be used at many operating conditions without having a need for altering the size of transistors. Also, the frequency

of operation is directly proportional to the bias current. Fig.3 shows the circuit of STCML inverter with two gate-drain connected

Fig.3 Circuit of STCML inverter



PMOS transistors in the pull-up and three NMOS transistors with one NMOS acting as current source in the pull-down. [4]

Total Delay is given as

$$t_d = \ln(2) \times C_L \cdot V_{sw}/I_{SS} \quad (2)$$

The Power-Delay product of the STSCL inverter is given as

$$PDP_{STCML} = \ln(2) \times C_L \cdot V_{sw} \cdot V_{DD} \quad (3)$$

C. ARM7 Organization

The Data path of ARM7 contains Address Register, Address Incrementer, Multiplier, Barrel Shifter, ALU, Write Data Register and Read Data Register all of 32-bit size. It also contains 31 ,32-bit registers in its Register Bank.[5],[6] The Block Diagram showing the Data path is in the Fig. 4. The Register bank of ARM7 can be operated in six modes:

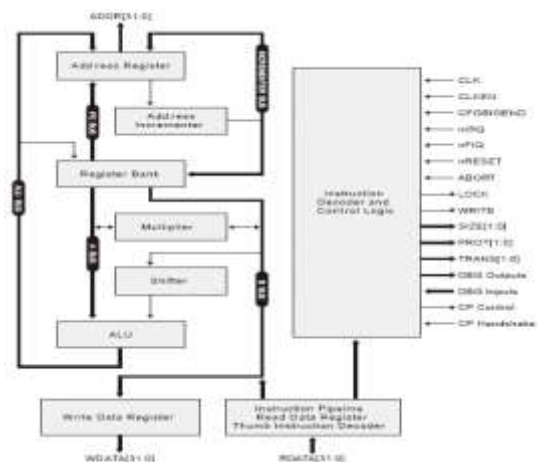


Fig.4 Block Diagram of ARM7

User mode, Supervisor mode, IRQ mode, FIQ mode, Abort mode and Undefined mode. The multiplier used in this paper for implementation of proposed Data path of ARM7 is 32x32

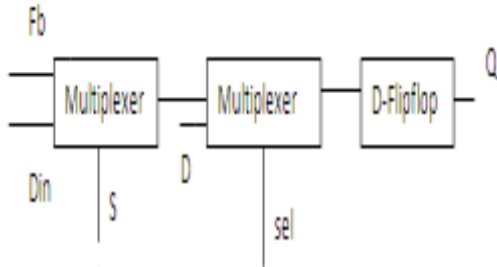


Fig 5 :primary cell of 32 Bit Address Register bit Vedic Multiplier. The ALU is of 32-bit and capable of performing a wide range of Arithmetic and Logic operations[6],[7]

Implementation of Datapath of Arm7 In STCML

The Datapath 32-bit ARM7 microprocessor has been implemented in Cadence Virtuoso in 45nm technology and with the power supply (V_{DD}) of 0.24V.

A. Address Register

The Block Diagram of 32-bit Address Register is as shown in Fig.5. The Address Register is used for storing the incremented address of the Program Counter. Its schematic contains Multiplexers and D-Flip flops.

B. Arithmetic and Logic Unit

The Block Diagram of 32-bit Arithmetic and Logic Unit (ALU) is as shown in the Fig.6. The proposed ALU is capable of performing 14 operations on 32-bit inputs $a<31:0>$ and $b<31:0>$. Table I shows the Arithmetic and Logical operations performed by the proposed ARM7.

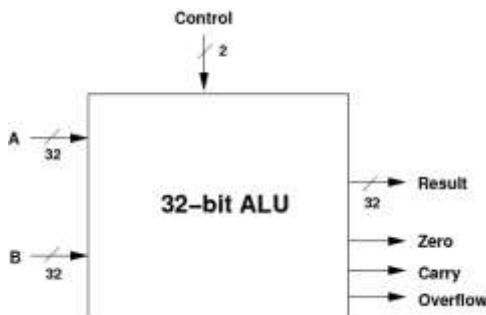


Fig. 6 Block Diagram of 32-bit ALU

The presented 32-bit ALU also sets the Zero, Carry and Overflow flags when the 32-bit result is all 0's,

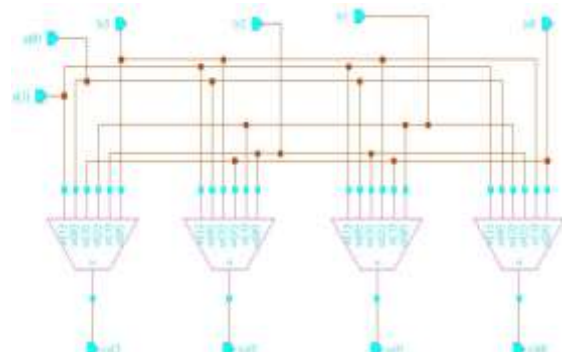
when there is a carry that is propagated or when the overflow condition has occurred. [6]

Table I Operations performed by the proposed 32-bit ALU

Sl.No.	Select line s	Output	Operation
1	1	out1<31:0>	Add Subtract
2		out2<31:0>	Logical AND
3		out3<31:0>	Bit Clear
4		out4<31:0>	Bit Invert
5		out5<31:0>	Increment
6		out6	Shift Left
7		out7	Rotate Left
8	0	out1<31:0>	Logical EXOR
9		out2<31:0>	carry_borrow
10		out3<31:0>	Logical OR
11		out4<31:0>	Compare if equal
12		out5<31:0>	Pass A input
13		out6	Shift Right
14		out7	Rotate Right

C. 32-bit Barrel Shifter

The schematic of 4-bit Barrel Shifter and the position of input bits after each shifting is as shown in the Fig.7 and Table II respectively. Barrel Shifter is used for shifting and rotating the input with the



help of Multiplexers. 32-bit Barrel Shifter consists of 32 multiplexers. [5]

Fig.7 Schematic of 4-bit Barrel Shifter

Select	Operation	Output
$s_1 s_0$		$out_3 out_2 out_1 out_0$
00	No rotation	$in_3 in_2 in_1 in_0$
01	Rotate left by 1 bit position	$in_2 in_1 in_0 in_3$
10	Rotate left by 2 bit positions	$in_1 in_0 in_3 in_2$
11	Rotate left by 3 bit positions	$in_0 in_3 in_2 in_1$

Table II A 4-bit Barrel Shifter Operation

The 32-bit Barrel Shifter has been designed using eight 4-bit Barrel Shifters. For rotating 4-bits, four 4x1 Multiplexers have been used. [5]

D. User Mode of ARM7

The User Mode facilitates the user to access all the registers in the Register Bank. It consists of r0-r7 General Purpose Registers and 5 Special Function Registers which are Current Program Status Register (CPSR), Saved Program Status Register (SPSR), Link Register (LR), Program Counter (PC) and Stack Pointer (SP).[6] The schematic of User Mode is shown in the Fig.8.

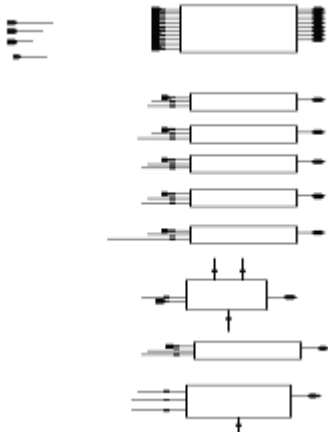


Fig.8 Schematic of User Mode

Also the schematic of 32-bit r0-r7 Registers is shown in the Fig.9. The registers used are 32-bit Parallel-In Parallel-Out Shift Registers (PIPO). All the other modes of ARM7 can be designed similarly by making use of these registers.

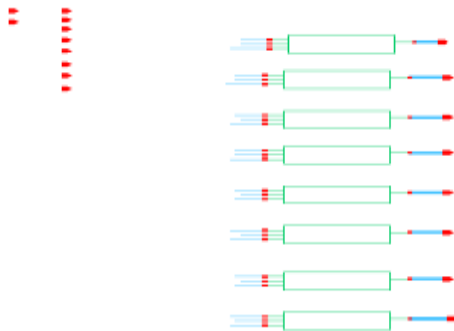


Fig. 9 32-bit r0-r7 general purpose registers

E. 32x32 Vedic Multiplier

The schematic of 2x2 Vedic Multiplier is shown in the Fig.10. The Vedic Multiplier is known for its quickness of multiplication and uncomplicated architecture. Not only in the processors, Vedic Multiplier has also been employed for ADSP and DSP applications. The schematic of 32x32 Vedic Multiplier includes four 16x16 Vedic Multipliers, two 32-bit Ripple Carry Adders and Half Adders.[8]

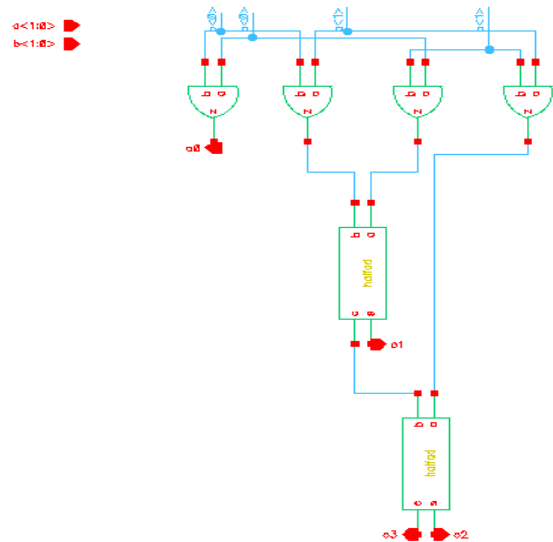
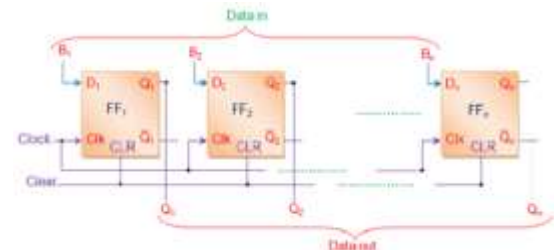


Fig.10 Schematic of 2x2 Vedic Multiplier

F. 32-bit Data-In Register

The Block diagram of N-bit Data-In Register is shown in the Fig.11. The 32-bit Data-In Register consists of 32 D-Flipflops connected in Parallel-In Parallel-Out manner.



The 32-bit Data-Out register is also designed in the same way like the 32-bit Data-In Register.

G. Data path Integration of ARM7 microprocessor

The complete schematic of Data path of ARM7 microprocessor can be viewed in Fig.12.

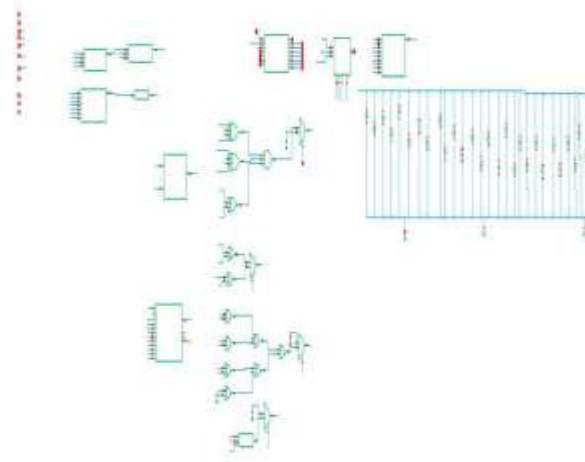


Fig.12: Schematic of Data path of ARM7 microprocessor

Results

The simulation results of all the blocks in the Data path of ARM7 have been observed in Spectre simulator. The inputs have a voltage of 0.24V as logic high or 1 and 0V as logic low or 0. All the results have been converted from Analog to Digital for ease of examining the output. The results of the Address Register are shown in the Fig.13. The inputs to it are 32-bit address and a feedback. The results of 32-bit ALU are shown in Fig.14 and 15. The outputs can be observed based on the select lines as shown in Table I of this paper. The outputs of the 32-bit Barrel Shifter are shown in Fig.16. The shifter takes 32-bit input and gives a 32-bit output after shifting and rotate operations are performed.

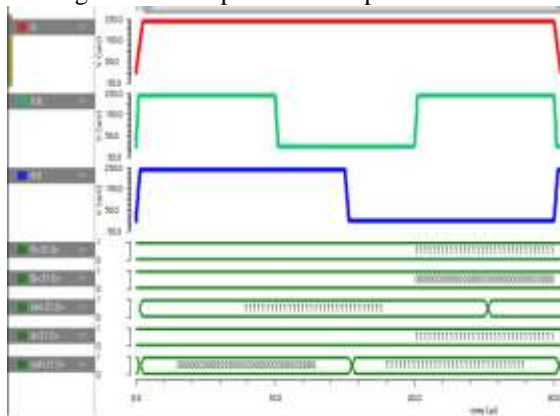


Fig.13: Simulation Results of 32-bit Address Register

When the select line Sel='0', out1<31:0> gives result of 32-bit addition/ subtraction, out2<31:0> gives result of Logical AND operation between the inputs a<31:0> and b<31:0>, out3<31:0> gives the output of Bit Clear operation, out4<31:0> gives the result after inverting all the bits of input a<31:0>, out5<31:0> gives the incremented output of input a<31:0>, out6 and out7 are shift left and rotate left outputs respectively.

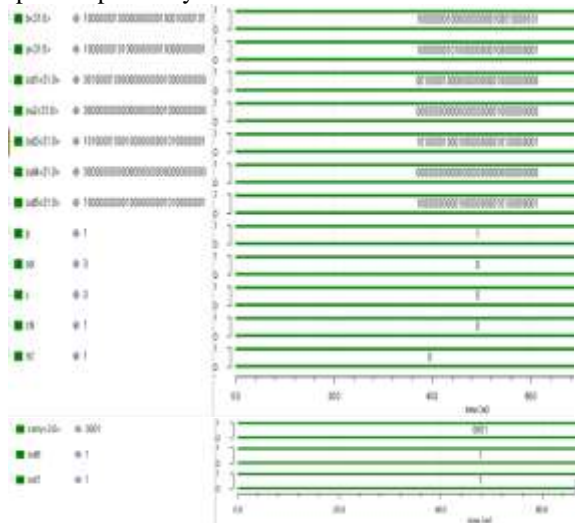


Fig.14: Results of ALU when select line is low

When the select line Sel='1', out1<31:0> gives results of Logical EXOR operation performed on inputs a<31:0> and b<31:0>, out2<31:0> gives carry/borrow bits of the 32-bit add/subtract operation, out3<31:0> gives logical OR operation output, out4<31:0> gives output for equality comparison of a<31:0> and b<31:0>, for out5<31:0> passes a<31:0> as it is, out6 and out7 are the results of shift right and rotate right respectively.

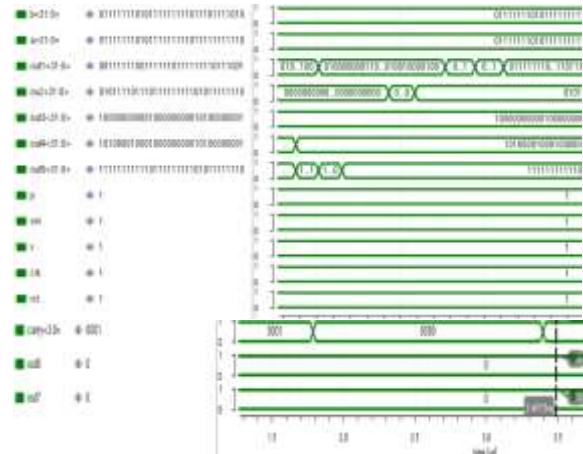


Fig.15 Results of ALU when select line is high.

The outputs of 32-bit Barrel shifter are shown in Fig.16. This shifted output is given to the 32-bit ALU for performing Arithmetic and Logical operations.

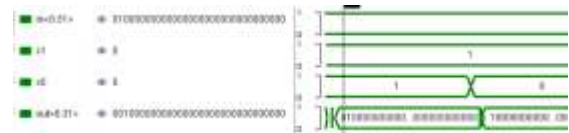


Fig.16 Results of 32-bit Barrel Shifter

The outputs of r0-r7 register bank z<0:255> are shown in Fig.17. The common input D<0:255> gets shifted into the registers eight registers which are each of 32-bit.

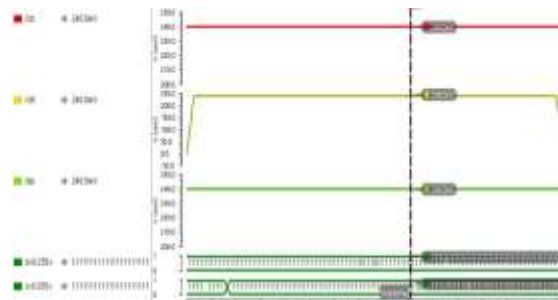


Fig.17 Results of Register Bank

The output of 32x32 Vedic Multiplier is as shown in the Fig.18. The inputs are a<31:0> and b<31:0> and the product is pr<63:0>



Fig.18 Results of 32x32 Vedic Multiplier

The results of 32-bit Data-In Register are shown in the Fig.19. The input is D<31:0> and output is z<31:0>.



Fig.19: Results of 32-bit Data-In Register

All the Data path components of ARM7 microprocessor have also been simulated at 0.5V power supply and the power and delay have been calculated. Table III and Table IV show the comparison of Power and Delay for the Data path components at 0.24V and 0.5V power supplies respectively.

Table III Power Comparison at Different Power Supplies

Design Block	STSCl at 0.24V Power Supply	STSCl at 0.5V Power Supply
32-bit Barrel Shifter	18.46x10 ⁻⁹ W	1.505x10 ⁻⁶ W
32-bit ALU	172.5x10 ⁻⁹ W	14.72x10 ⁻⁶ W
Register Bank	479x10 ⁻⁹ W	43.51x10 ⁻⁶ W
32x32 Vedic Multiplier	386.4x10 ⁻⁹ W	78.02x10 ⁻⁶ W
32-bit Data-In Register	10.79x10 ⁻⁹ W	942.8x10 ⁻⁹ W
32-bit Data-Out Register	10.68x10 ⁻⁹ W	940.2x10 ⁻⁹ W
32-bit Address Register	23.56x10 ⁻⁹ W	680.4x10 ⁻⁹ W
32-bit Address Incrementer	5.34x10 ⁻⁹ W	575.4x10 ⁻⁹ W

Table IV Delay Comparison at Different Power Supplies

Design Block	STSCl at 0.24V Power Supply	STSCl at 0.5V Power Supply
32-bit Barrel Shifter	20.82us	20.17us
32-bit ALU	25.68us	9.79us
Register Bank	439.1ns	173.4ns
8-bit RCA	56.9us	51.25ns
32x32 Vedic Multiplier	658.4us	19.29us
32-bit Data-In Register	890us	465.2ns
32-bit Data-Out Register	887.5us	459.8ns
32-bit Address Register	27.9us	347.7ns
32-bit Address Incrementer	89.2us	25.04us

Conclusion

This paper presents an innovative power efficient methodology for the design of Data path components of ARM7 microprocessor using Cadence Virtuoso in 45nm technology with 0.24V power supply. It can be inferred from the power calculations that when the voltage scaling is done the power consumption has reduced without causing any effect in the correctness of the waveforms. Also, this method has proved to be efficient for the design of ARM7 and also created room to incorporate the Sub threshold Current Mode Logic with other low power logics in order to reduce the power consumption further if desired.

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