

Five level inverter with SVPWM Control Technique

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Abstract

This paper provides the proposed single phase five level inverter with Dc link Switches based on SVPWM technique. This paper focuses on improving harmonic performance of the multilevel inverter and quality of output voltage waveform compared to conventional two-level inverter. It uses two carrier wave and three reference waves which are generated from SVPWM technique. The whole system is implemented using MATLAB/Simulink. The inverter is connected to R-load, RL-load and performances are analyzed.

Keywords: Multilevel Inverter, SVPWM technique (Space Vector Pulse Width Modulation), Sector, Alfa, Beta, THD.

Introduction

The Multilevel inverter topologies are the best suited for medium and high voltage applications in the industries. Now a day's tremendous interest were drawn in the power industry as this inverter exclusively used in increased power rating, reduced THD and reduced EMI. The switching losses are almost negligible because these are switched at low switching frequency compared to conventional multi-level inverters. To endure with associated problems with the two level inverter, multilevel inverters (MLIs) are introduced [1]. The inverter should have the appropriate requirements.

- Inverter output current should have low total harmonic distortion (THD).
- To generate a pure sinusoidal output voltage

The output filter, inductor must have suitable value to satisfy the appropriate THD value in conventional two level inverter, hence MLIs are introduced for industries and also for grid connected applications [2-4].

The types of multilevel inverters are:-

- Diode clamped multi level inverter.
- Cascaded H bridge multi level inverter.
- Flying capacitor type multi level inverter.

Because of development of power electronic devices like MOSFET, IGBT and SCRs etc... There is a tremendous advance in power electronic converters this made the multilevel inverters concept practical in industries. The thought

of multi-level inverter has become superior advantageous so that several major manufacturers have obtained patents on multi-level power electronic converters. The multilevel inverter will have dominant features in future coming years, particularly in high power applications.

The applications of multi-level inverter are variable speed drives, Power factor control, reactive power compensation, etc. [5-7]. The Physical structure of Multi level inverters must have the ability to withstanding high input voltages for high power applications. So, A new topology which is capable to scale down the problems faced by the conventional two-level inverter [8].

The advantages of multi-level inverter over the conventional two level inverter is that, the proposed multi-level inverter has less number of switch count. The THD of the proposed multi-level will be less compared to conventional two-level inverter. The most important concept is that the DC-link capacitor voltage must have equally balanced. If it is not balanced equally the output voltage becomes unsymmetrical and it leads to high harmonic content in the load voltage and load current.

The proposed multilevel topology is controlled with carrier based Pulse Width Modulation techniques. So many techniques were proposed in the literature among them the following are the famous CB-PWM.

1) Phase disposition (PD): In this Phase Disposition technique all the carrier waves are in phase with each other

2) Alternative phase opposition disposition (APOD): In which all the carrier waves are phase shifted by 180° with the adjacent carrier wave.

3) Phase opposition disposition (POD): In this technique, above the zero voltage carrier waves are 180° out of phase with those carrier waves below zero voltage.

4) Space Vector Pulse Width modulation: In this technique it under goes a method, The sector in which it consists of eight states in which two states were in valid. This technique uses volt-sec balance.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed inverter consists of eight switches and two DC-link symmetrical capacitors C_1 and C_2 . The inverter supply is U_{dc} and due to the capacitors the voltage will divide into two half i.e., $U_{dc}/2$. Fig: A

shows the proposed five-level inverter topology. Table A shows switching sequence to produce five-level output.

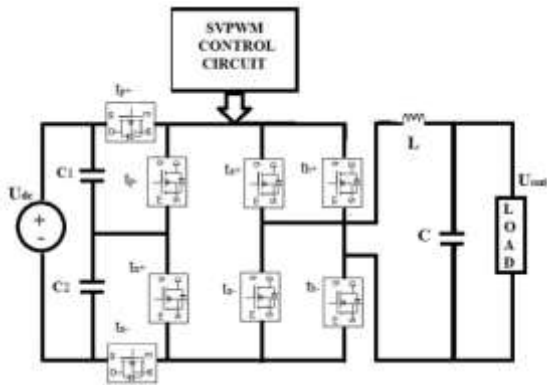


Fig: A. five-level multi-level inverter topology

Specifications of proposed inverter topology are as follows:

- Input DC voltage (U_{dc}) = 100 v
- Output Voltage (U_0) = 50 v (rms)
- Filter inductance (L) = 300 μ H
- Filter capacitance (C) = 150 μ F
- Resistive load (R) = 10 ohms
- Inductive load (L) = 10 mH

TABLE: A. SWITCHING SEQUENCE

U_{out}	Switching conditions							
	t_p^+	t_p^-	t_n^+	t_n^-	t_a^+	t_b^-	t_a^-	t_b^+
U_{dc}	ON	OF	OF	ON	ON	ON	OF	OFF
$U_{dc}/2$	OF	ON	OF	ON	ON	ON	OF	OFF
$U_{dc}/2$	ON	OF	ON	OFF	ON	ON	OF	OFF
0	OF	ON	ON	OFF	ON	ON	OF	OFF
0	OF	ON	ON	OFF	OF	OF	ON	ON
$-U_{dc}/2$	OF	ON	OF	ON	OF	OF	ON	ON
$-U_{dc}/2$	ON	OF	ON	OF	OF	OF	ON	ON
$-U_{dc}$	ON	OF	OF	ON	OF	OF	ON	ON

SVPWM CONTROL TECHNIQUE

In the trends of SVPWM the development of the reference voltage vector (U_{ref}) is obtained by using the volt-second balance. The voltage vector U_{ref} can be calculated by using adjacent voltage vector in a sector of the hexagon figure [9].

U_{ref} can be given by,
 $U_{ref} = t_n U_{mn}/t + t_{n-1} U_{mn-1}/t + t_0 U_0/t + t_7 U_7/t$ (1)

Where t = switch period, t_n, t_{n-1} are operating time of U_{mn}, U_{mn-1} respectively. t_0, t_7 are operating time of U_0, U_7 respectively.

t and U_{ref} can be calculated by using hexagon figure Fig: B.

$t = t_1 + t_3 + t_0$
 $U_{ref} = t_1 U_0 / t + t_3 U_3 / t.$ (2)

Where t = carrier wave time period t_1, t_3 are time period of U_0, U_3 respectively.

The voltage ref vector can be expressed by using a reference frame *alfa-beta* and can be given as,

$U_{alfa} = t_1 U_0 / t + t_3 U_3 \cos(\pi/3) / t_0$
 $U_{beta} = t_3 U_3 \sin(\pi/3) / t$ (3)

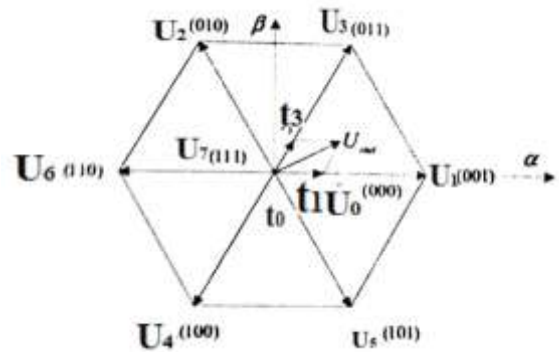


Fig: B. Space vector hexagon figure

$t_1 = 3t U_{alfa} / 2U_{dc} - \sqrt{3} t U_{beta} / 2U_{dc}$
 $t_3 = \sqrt{3} t U_{beta} / U_{dc}$
 $t_0 = t - t_1 - t_3$ (4)

The reference frame voltage vectors U_{alfa} and U_{beta} are given then t_1 and t_3 can be calculated. suppose $t_2 = t_3$, operating times t_{aon}, t_{bon} and t_{con} can be given as

$t_{aon} = (t - t_1 - t_2) / 4$
 $t_{bon} = (t_{aon} + t_1) / 2$
 $t_{con} = (t_{bon} + t_2) / 2$ (5)

In the same way the time period of t_n, t_{n-1} can be calculated [10].

SIMULATION MODELING AND RESULTS

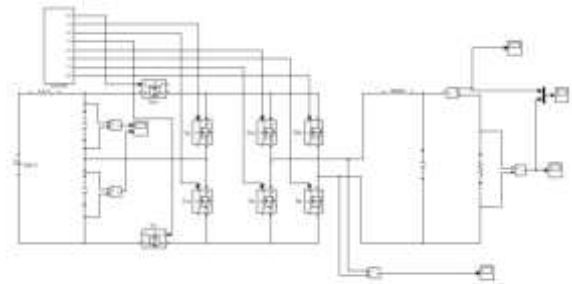


Fig: C. simulation model for multi-level topology with R load.

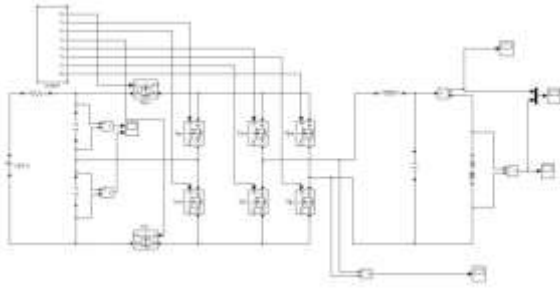


Fig: D. simulation model for multi-level topology with RL-load

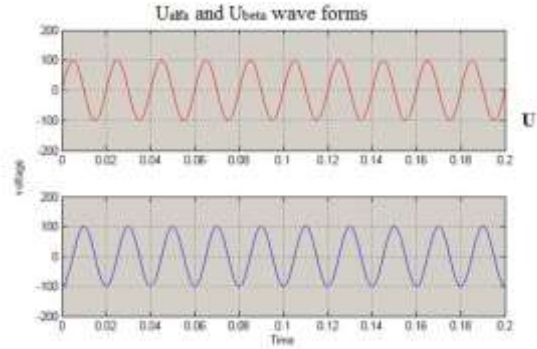


Fig: H. Simulation results of U_{α} and U_{β}

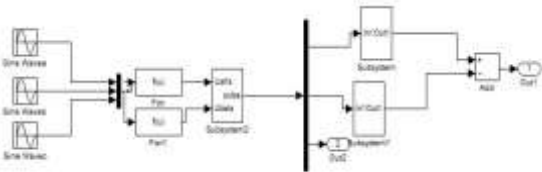


Fig: E. simulation model for SVPWM
The three sine wave which are displaced by the 120° phase shift with 100v amplitude, the three sine waves are given to mux and this mux output converted to alpha and beta by using functional block. The alpha & beta were given to the subsystem2 in which required pulses are generated.

1) Model for calculating U_{ref}

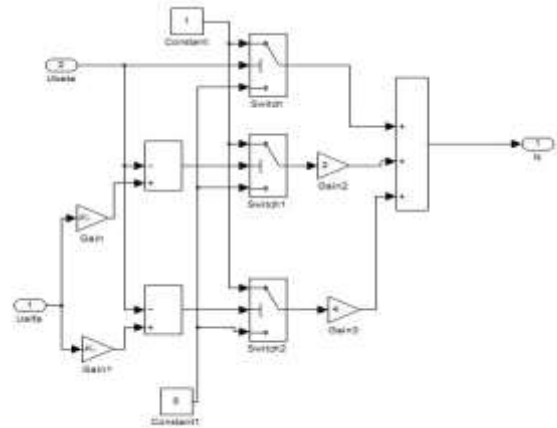


Fig: I. simulation model for U_{ref}

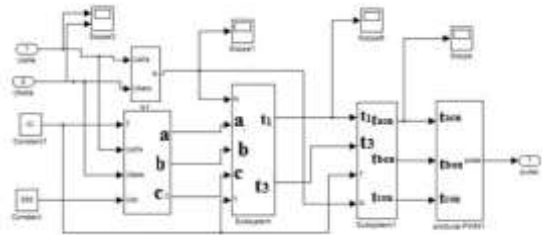


Fig: F. simulation model for sub system2 in Fig: E.

The section number of U_{out} can be calculated as $N = 4 \times c + 2 \times b + a$

Where,

a is output of block (switch)

b is output of block (switch1)

c is output of block (switch2)

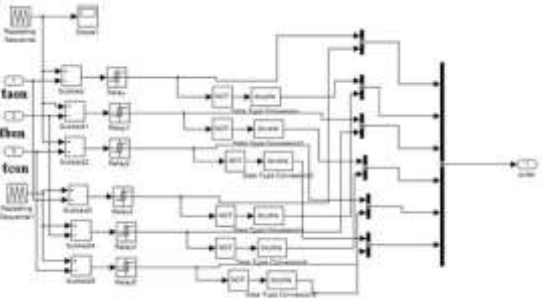


Fig: G. simulation model for producing t_{p^+} , t_{p^-} , t_{n^+} , t_{n^-} , t_{a^+} , t_{b^-} , t_{a^-} , t_{b^+} .

The t_{aon} , t_{bon} and t_{con} are compared with the high frequency carrier signal to generate required pulse, in which nearly 12 pulses are generated but for proposed multilevel inverter there are 8 switches they require only 8 pulses for that purpose certain subsystem is developed.

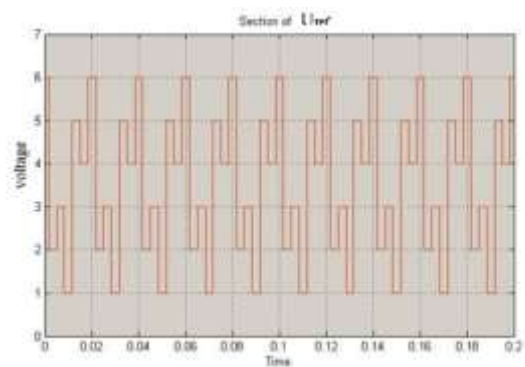


Fig: J. simulation result of U_{ref}
2) Modeling for finding out t_1 and t_3

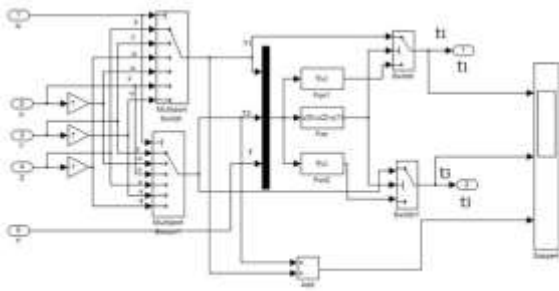


Fig: K. simulation model for t_1 and $t_3(4)$

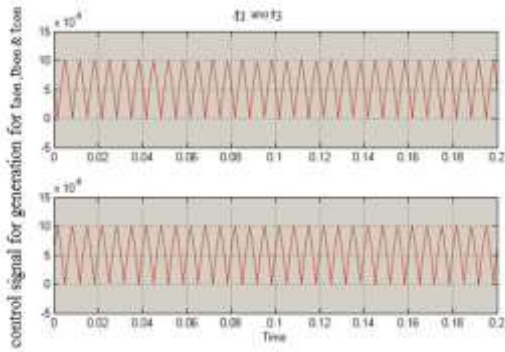


Fig: l. simulation result of t_1 & t_3

3) Modeling for t_{aon}, t_{bon} & t_{con}

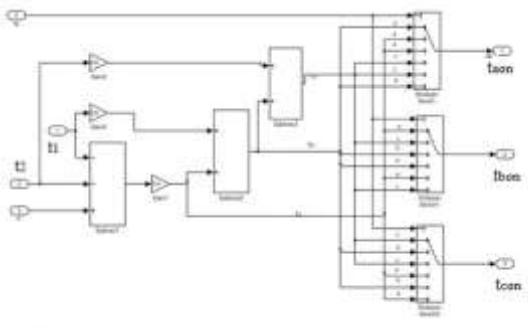


Fig: M. simulation model for t_{aon}, t_{bon} & $t_{con}(5)$

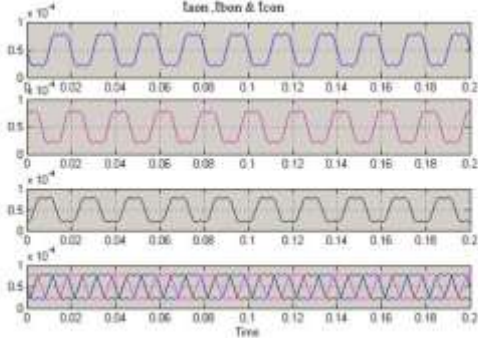


Fig: N. simulation result of t_{aon}, t_{bon} & t_{con}

4) Simulation results of the proposed multi-level topology

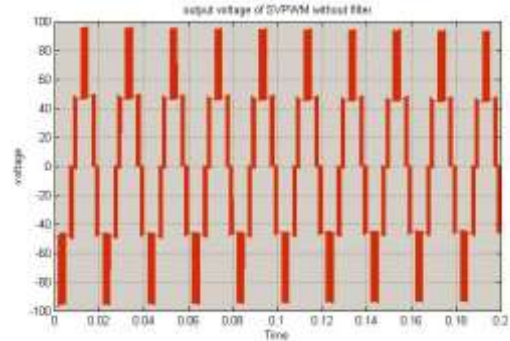


Fig: O. output voltage of the proposed multi-level inverter topology without filter

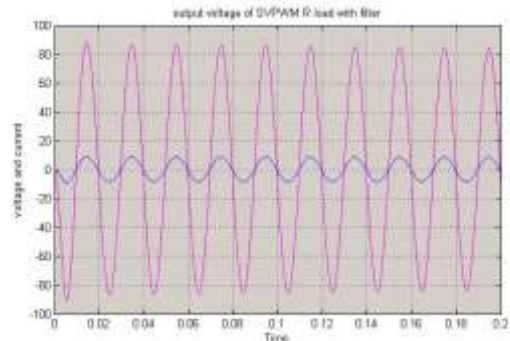


Fig: P. simulation result of output voltage of SVPWM for R load with filter

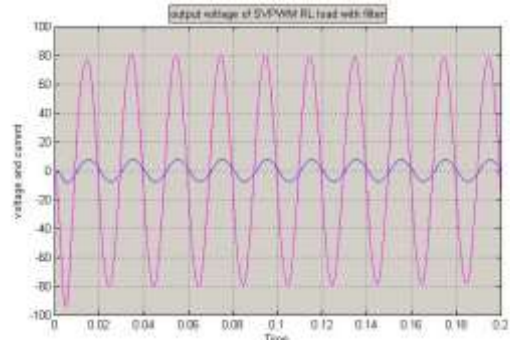


Fig: Q. simulation result of output voltage of RL-load with filter

The simulation output voltage results in Fig: P&Q says that the output wave forms are somewhat better, with improved pureness of waveforms.

5) Voltage THD of R-load and RL-load

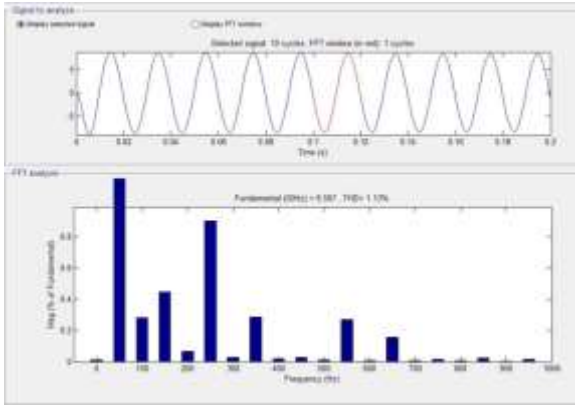


Fig: R. THD of Five level inverter using SVPWM for R load

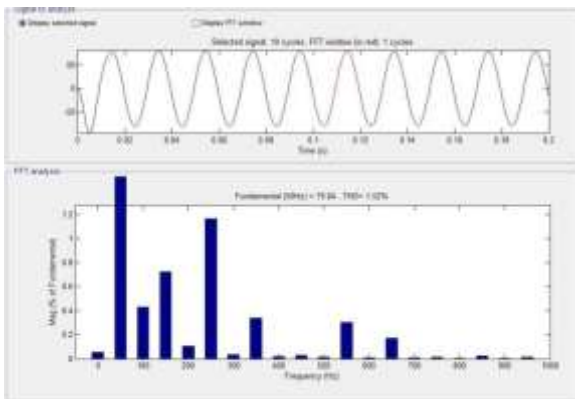


Fig: S. THD of Five level inverter using SVPWM for RL load

From the above FFT analysis the total harmonic distortion for R load 1.13% and RL load 1.52% as the percentage values of THDs are less than 5% , reduced THDs are obtained compared to conventional multi-level inverters.

Conclusion

The Five level inverter Topology using Space Vector pulse width modulation technique is implemented in MATLAB/Simulink. U_{ref} obtained by using *alfa-beta* reference frame. The total harmonic distortion is quite low as compared to conventional multi-level inverter. The switches count reduced, besides that the output voltage is nearly pure sinusoidal that means the quality of the wave form is improved.

The result with R and RL load has evaluated. By observation it is seen that the voltage THD of proposed multilevel inverter with RL-load has little high THD compared to R load i.e., 1.52% & 1.13% respectively.

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