

Design Analysis of SRAM Cell with Improved Noise Margin based on Aspect Ratio Adjustments

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Abstract

Due to increasing demand for faster memory devices, SRAM has gained importance for research focus. SRAM cells have various applications like SRAM based LUT in FPGA, DSP applications, electronic subsystems of telecommunications etc. As the technology scales down the threshold voltage is lowered, leading to less margin to noise and disturbs the SRAM cell stability. The proposed work investigates on the CMOS based memory cell in submicron regions analyzing the static noise margin during active operations and improves the cell stability.

Keywords: 6T SRAM, Static Noise Margin, Read Margin, Write Margin, Hold Margin.

Introduction

The SRAM cell stability determines the soft-error rate and the sensitivity of the memory to process tolerances and operating conditions. To analyze static cell stabilities Static Noise Margin (SNM) simulations have become dominant method to assess the cell reliability in high density memories [1]. The focus of cell stability on SNM analyses of SRAM cells have mostly restricted to the simulations, however, some works discuss this through providing analytical expression [2,9]. This work deals with the SNM of SRAM cell both from analytic as well as simulations point of view. The advantage of mathematical representation is that it explicitly expresses the SNM as function of different cell parameters such as supply voltages, pre-charge voltages, bit line voltages, and source voltages.

A. 6T SRAM Cell

6T SRAM cell, as the name indicates it consists of 6 transistors in which two are pull-up transistors, two are pull-down transistors and two are access transistors. These two pull-up and pull-down transistors are together formed into two cross coupled inverters on which each bit of information is stored. The 6T SRAM occupies least area on a chip as it has less number of transistor with the least average rise time and fall time [5]. The two access transistors are connected to two bit lines (BL and BLB) and a word line (WL) as shown in fig. 1.

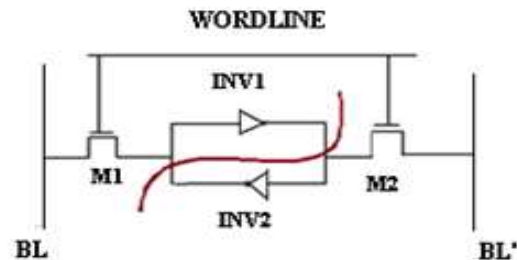


Fig. 1. Basic 6T SRAM cell with two back to back inverters

The accesses to a storage cell during read and write operations is served by the two access transistors. The word line enables the access to the cell.

B. READ OPERATION

To perform read operation pre charge both the bit lines i.e, BL and BLB to high and then turn on the word line(WL). The bit lines will be pulled down to low depending on the node voltages present at node Q and QB. For instance assume that Q=0 and QB=1 Then the bit line BL discharges through the transistors M5 and M1 to ground and the bit line BLB remains high, but the voltage at node Q slightly bumps up. In order for node Q not to flip its state, the transistor M1 should be stronger than the transistor M5 i.e, $M1 \gg M5$.

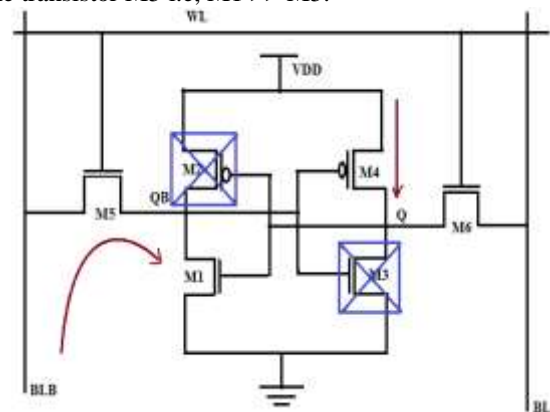


Fig. 2. Basic circuit diagram for 6T SRAM cell read operation

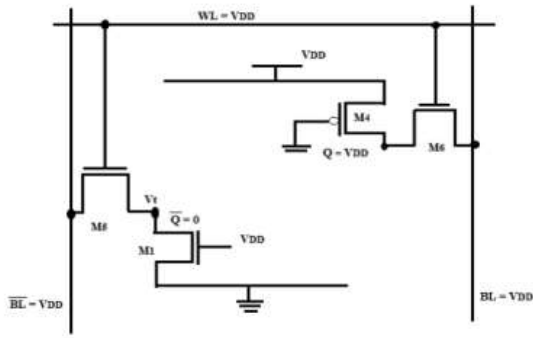


Fig. 3. Circuit diagram showing read operation of 6T SRAM cell

Modeling for Current Equations during Read Operation

Figure 3 illustrates the region of operation during read. When the voltage at Q-bar node reaches the threshold voltage of the NMOS i.e, M3, the voltage at node Q starts to decrease and regenerative action of the cross coupled inverter will force the flipping of the bit in the cell. Since the transistor M6 is in cut-off region, the current takes the path through transistors M5 and M1. Hence the currents of M5 and M1 are equal. ID5 and ID1 represent the currents at M5 and M1 respectively.

The equation which represents the read operation is as follows

$$I_{D5} = (\beta_{n5}/2)(V_{DD} - V_1 - V_{tn})^2 \tag{1}$$

$$I_{D1} = (\beta_{n1}/2)(2(V_{DD} - V_{tn})V_1 - V_1^2) \tag{2}$$

Equating (1) and (2), we get

$$I_{D5} = I_{D1} \\ (\beta_{n5}/2)(V_{DD} - V_1 - V_{tn})^2 = (\beta_{n1}/2)(2(V_{DD} - V_{tn})V_1 - V_1^2) \tag{3}$$

Where V_{DD} = Power supply

V_{tn} = Threshold voltage at NMOS transistor

β = Cell ratio(W/L(NMOS)/W/L(Driver Transistor))

C. WRITE OPERATION

To perform write operation, initially turn on the word line (WL) and the value which is to be written is given to the bit lines i.e if we wish to write 0 then we would apply 0 to the bit line BL and 1 to bit line BLB and vice versa in case if we wish to write 1, then the value to be stored is get latched in.

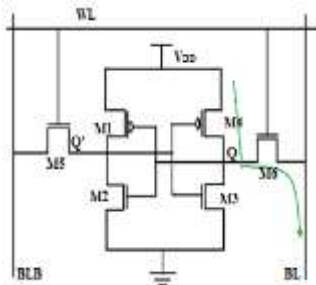


Fig. 4. Basic circuit diagram for 6T SRAM cell write operation

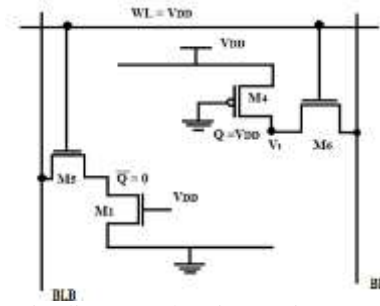


Fig. 5. Circuit diagram showing write operation of 6T SRAM cell

Modeling for Current equations during write operation

Figure 5 illustrates the region of operation during write. When the voltage at node Q reaches below the threshold voltage then the PMOS i.e, M2 gets on, the voltage at node Q bar starts to increase and the regenerative action of the cross-coupled inverter will force to write 'Q' as '0'. Since the transistor M6 is in linear region, the current takes the path through M4 and M6. Hence the currents of M4 and M6 are equal. The current at M4 and M6 is represented as ID4 and ID6 respectively.

The equation which represents the write operation [1] is as follows

$$I_{D4} = (\beta_{p4}/2)(V_{DD} - V_{TP})^2 \tag{4}$$

$$I_{D6} = (\beta_{n6}/2)(2(V_{DD} - V_{TN})V_1 - V_1^2) \tag{5}$$

Equating (4) and (5)

$$I_{D4} = I_{D6} \\ (\beta_{p4}/2)(V_{DD} - V_{TP})^2 = (\beta_{n6}/2)(2(V_{DD} - V_{TN})V - V_1^2) \tag{6}$$

Where V_{DD} = Power supply

V_{TP} = Threshold voltage at M4

V_{TN} = Threshold voltage at M6

β = Pullupratio(W/L(AccessTransistor)/W/L(PMOS))

D. HOLD OPERATION

To perform the hold operation, turn off the word line (WL). If the word line is not asserted, the access transistors disconnect the cell from the bit lines. The two cross coupled inverters formed will continue to reinforce each other as long as they are connected to the supply [2].

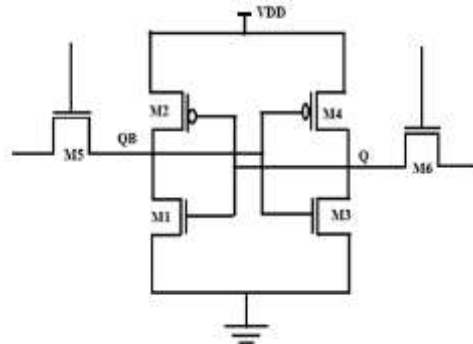


Fig. 6. Circuit diagram showing hold operation for 6T SRAM cell

Two aspects are important for SRAM cell design are the cell area and the stability of the cell. The cell area determines about two-thirds of the total chip area. The cell stability determines the soft-error rate and the sensitivity of the memory to process tolerances and operating conditions [1].

Various architectures of SRAM cells are simulated which include 6T, 7T, 8T and 9T cells and drawn conclusion that despite of high layout area, it is found that 9T cell has high data stability with low power requirements in exchange with performance [7]. Since memory designs are mainly categorized in terms of area, speed and power. The power dissipation of 8T SRAM is twice the power dissipation in 6T SRAM. This is due to higher number of transistors and little higher working complexity than the other [3].

As we go from one SRAM cell to another the design can be optimized by trade-off between various parameters like power consumption, delay, chip area etc. when compared to other configurations 10T SRAM consumes the least amount of power and has less delay but it occupies large area as it contains more number of transistors[4,6].

A new 6T SRAM cell was designed for low power by using separate bit and word lines which improved noise margins in nano scale technology but the yield has a considerable effect.[6] A traditional 6T SRAM cell is preferred for the static noise margin analysis is performed during read, write and hold operations in submicron regions. [1]. A read, write and hold SNM are modeled by varying various parameters like cell ratio, pull up ratio, temperature, supply voltage and process corner variations. [2]Improving the noise margin by analyzing the parameters affecting read, write and hold SNM is proposed graphically and analytically in view of performance metric which is very vital in memory based systems.

II. WRITE STATIC NOISE MARGIN

Static noise margin (SNM) is the key factor for an SRAM cell. The lower supply voltage by which the stability of the SRAM depends can be measured by static noise margin [8]. Write noise margin is defined as the lower bit line voltage than the power supply voltage VDD that is required for flipping the state of SRAM. The bit line that is charged to '0' pulls the node of the cell storing '1' to '0' causing the cell to flip state[6].

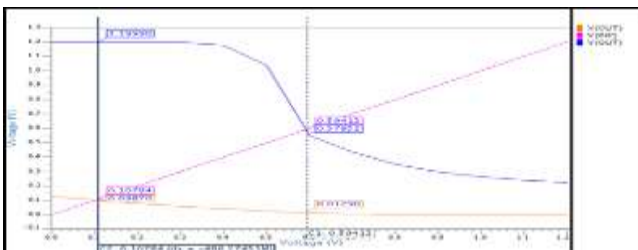


Fig.7. VTC curve for WSNM characteristics

Write failure occurs if the node storing '1' cannot be discharged through the access transistors when the word line is set to high. To prevent the write failure the driver current of the access transistor should be more than the driver transistor. The

condition that is to be followed to obtain stable write is given by Eq. (8)

$$\mu_{n}c_{ox}(W_{d}/L_{d})(V_{wl}-V_{th,d})^{\alpha} >> \mu_{p}c_{ox}(W_{p}/L_{p})(V_{cell}-V_{th,p})^{\alpha} \quad (8)$$

Where μ = mobility

W_{p}/L_{p} = ratio between width to length of PMOS transistor

α = switching factor

W_{a}/L_{a} = between width to length of access transistor

C_{ox} = channel capacitance

III. READ STATIC NOISE MARGIN

It is defined as the maximum value of DC noise voltage that can be tolerated by SRAM cell without changing the stored bit[2]. The SNM of a 6T SRAM cell can be determined by using a model as shown

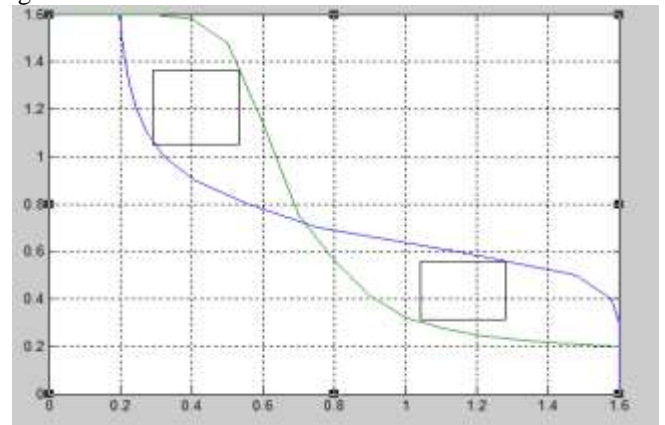


Fig. 8. VTC curve for RSNM characteristic

Read failure occurs when the voltage V₀ at node 'Q' raises, then the transistor M5 becomes more and more resistive which leads the whole data to swing. To prevent the read failure the driver current of the driver transistor should be more than the access transistor. The condition that is to be followed to obtain stable read is given by Eq. (9)

$$\mu_{n}c_{ox}(W_{d}/L_{d})(V_{cell}-V_{th,d})^{\alpha} >> \mu_{p}c_{ox}(W_{a}/L_{a})(V_{wl}-V_{th,a})^{\alpha} \quad (9)$$

Where μ = mobility,

W_{d}/L_{d} = ratio between width to length of driver transistor

α = switching factor

W_{a}/L_{a} = between width to length of access transistor

C_{ox} = channel capacitance

IV. HOLD SNM

The two cross coupled transistors formed will continue to reinforce each other as long as they are connected to power supply. If the word line not asserted to the access transistor, disconnects the cell from the bit lines[2].

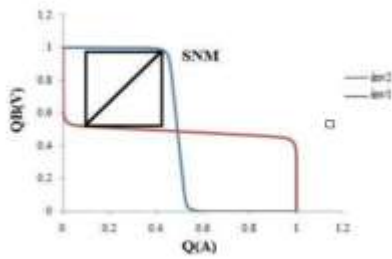


Fig. 9. General SNM characteristics during hold

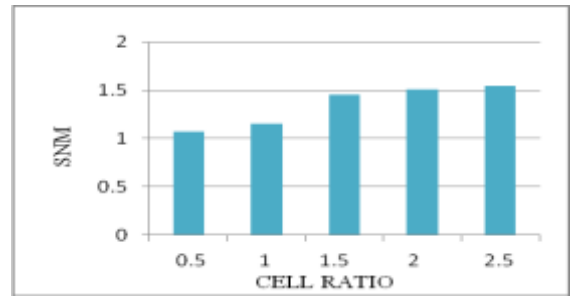


Fig.17.Effect of RSNM for different cell ratio at 2.5v

The improvement in SNM is clearly observed in the below figure with the variation in different voltages.

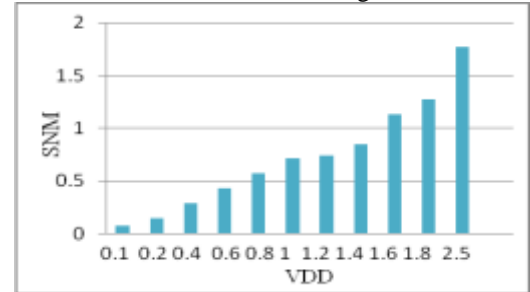


Fig. 12. Hold noise margin for different supply voltages

The simulation graphs for various pull up ratios for 6T SRAM cell Write '0' operation at 2.5 supply voltage are as follows

Results

The improvement in SNM is clearly observed in the below figure with the variation in different pull up ratios. The graph is drawn for different pull up ratios at 2.5 voltage supply.

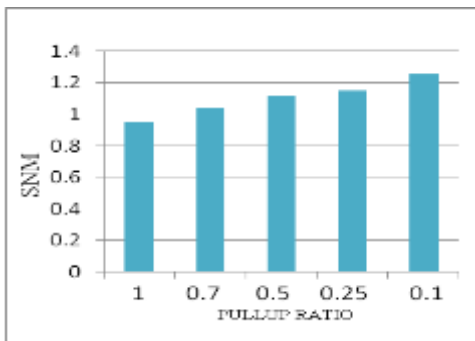


Fig. 10. Effect of WSNM(write 0) for different pull up ratio at 2.5v

The improvement in SNM is clearly observed in the below figure with the variation in different pull up ratios. The graph is drawn for different pull up ratios at 2.5 voltage supply.

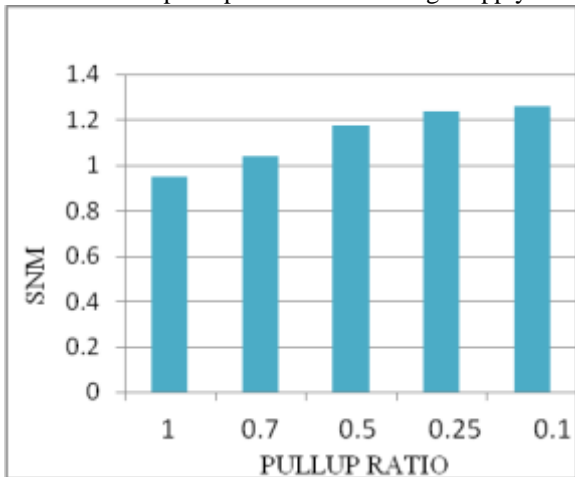
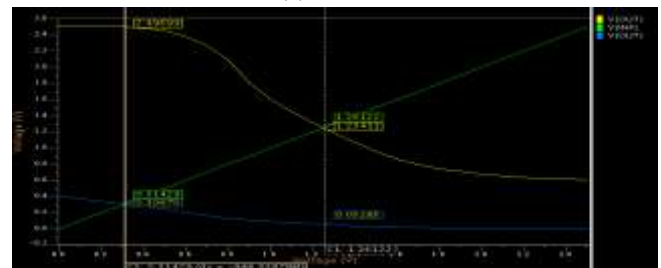


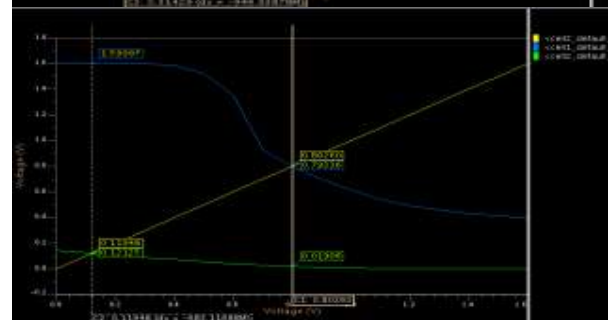
Fig. 11. Effect of WSNM(write 1) for different pull up ratio at 2.5v

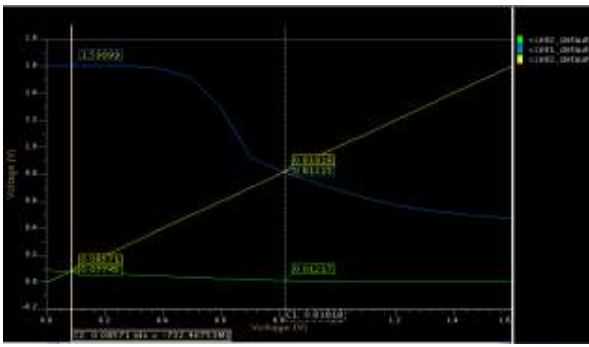
The improvement in SNM is clearly observed in the below figure with the variation in different cell ratios. The graph is drawn for different cell ratios at 2.5 voltage supply.

(a)

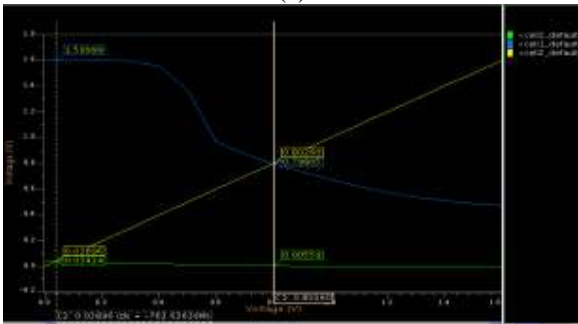


(b)





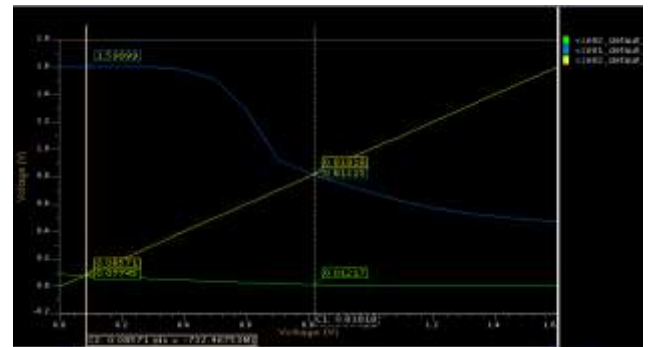
(c)



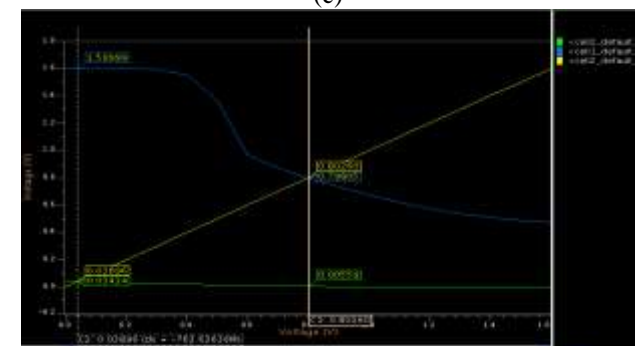
(d)

Fig. 13. Write Static Noise Margin (Write 0) of 6T SRAM cell for 2.5V (a) at 1 ratio(b) at 0.7 ratio (c) at 0.5 ratio (d) at 0.25 ratio

The simulation graphs for various pull up ratios for 6T SRAM cell Write '1' operation at 2.5 supply voltage are as follows



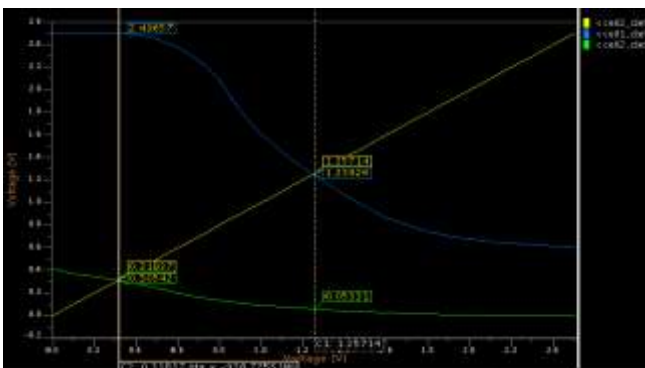
(c)



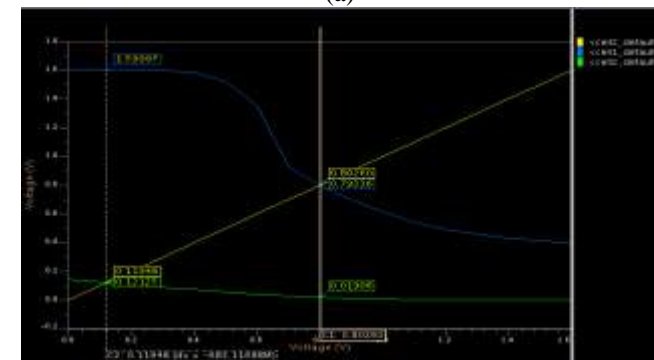
(d)

Fig. 14. Write Static Noise Margin (Write 1) of 6T SRAM cell for 2.5V (a) at 1 ratio(b) at 0.7 ratio (c) at 0.5 ratio (d) at 0.25 ratio

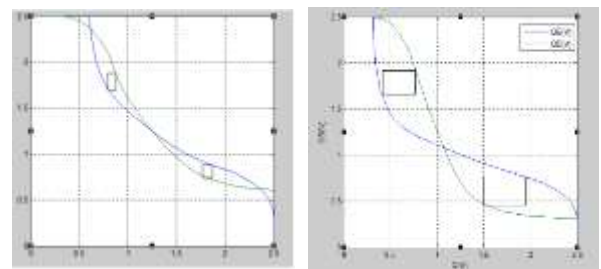
The simulation results for read SNM for various cell ratios, obtained using matlab at 2.5 supply voltage are as follows.



(a)

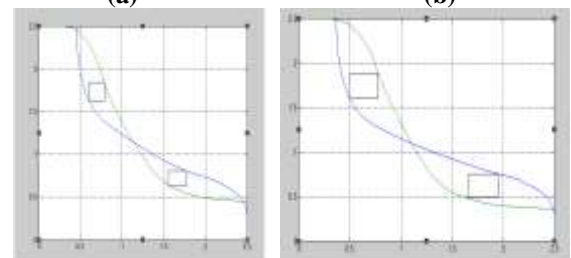


(b)



(a)

(b)



(c)

(d)

Fig. 15. Read Static Noise Margin (RSNM) of 6T SRAM cell for 2.5V (a) at 0.5 ratio(b) at 1 ratio (c) at 1.5 ratio (d) at 2 ratio.

Integrated circuit layout, also known as IC layout or IC mask layout is the representation of an integrated circuit in terms of geometric shapes. The layout diagram, for 6T SRAM cell is as follows.

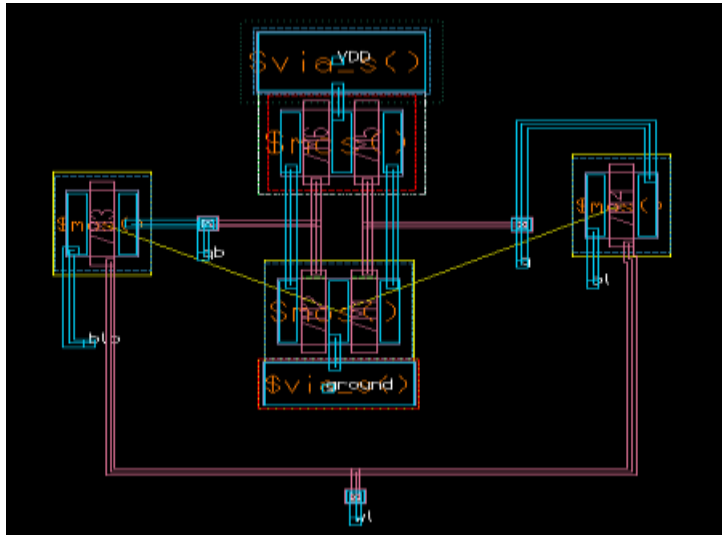


Fig. 16. 6T SRAM cell layout

The simulation results for 6T SRAM cell layout that is both post layout and pre layout simulation waveforms are as follows.

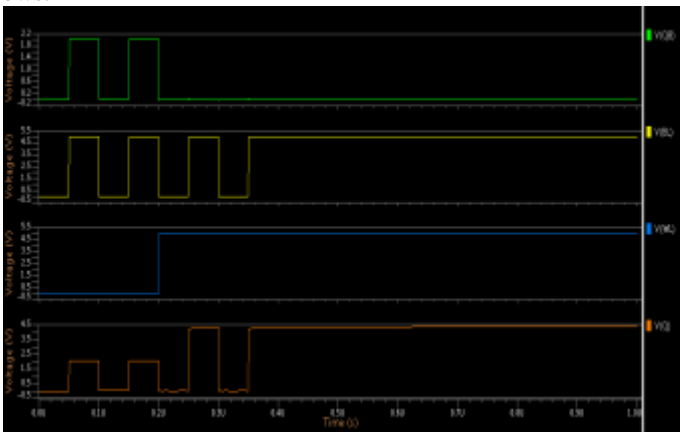


Fig. 17. Pre layout of 6T SRAM cell.

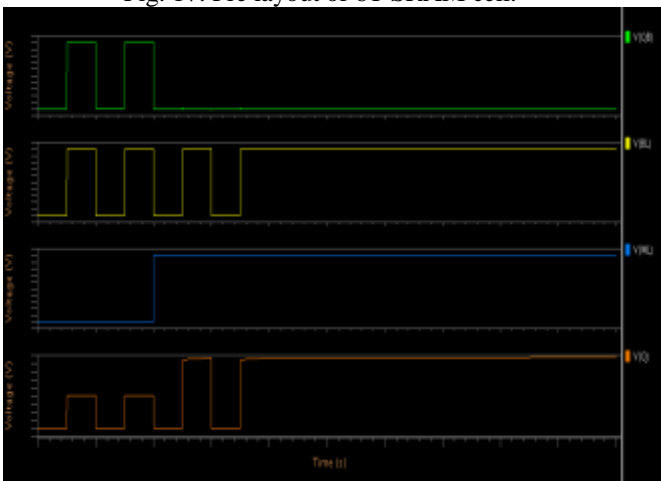


Fig. 18. Post layout of 6T SRAM cell.

Conclusions

Nano scaled technologies for low power and high speed applications degrades the stability which is measured by static noise margin. From the above analysis, it can conclude that the reliability of 6T SRAM cell can be effected with operating supply, pull up ratio and cell ratio. At different variation in cell ratio and pull up ratio the RSNM and WSNM has improved at dynamic supply voltages. This shows that the 6T SRAM cell operate efficiently in sub threshold regions.

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